

Compal Confidential

PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

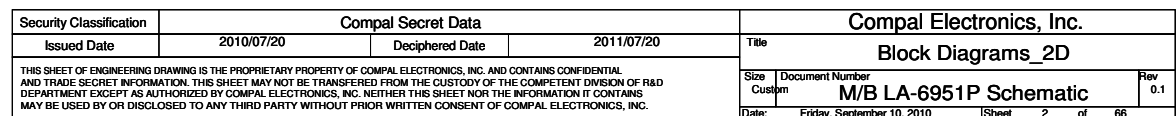
AIO M/B

2010-09-10

REV: 0.1

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File Name : LA6951P



Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	N/A	N/A	N/A
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@ (VRAM:Hynix)
0	1	0	DIS@ (VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
EHCI2	UHCI3	6	USB 2.0
		7	3D IR
	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(TV Tuner)
	UHCI6	12	Mini Car(WLAN)
		13	

BTO Option Table

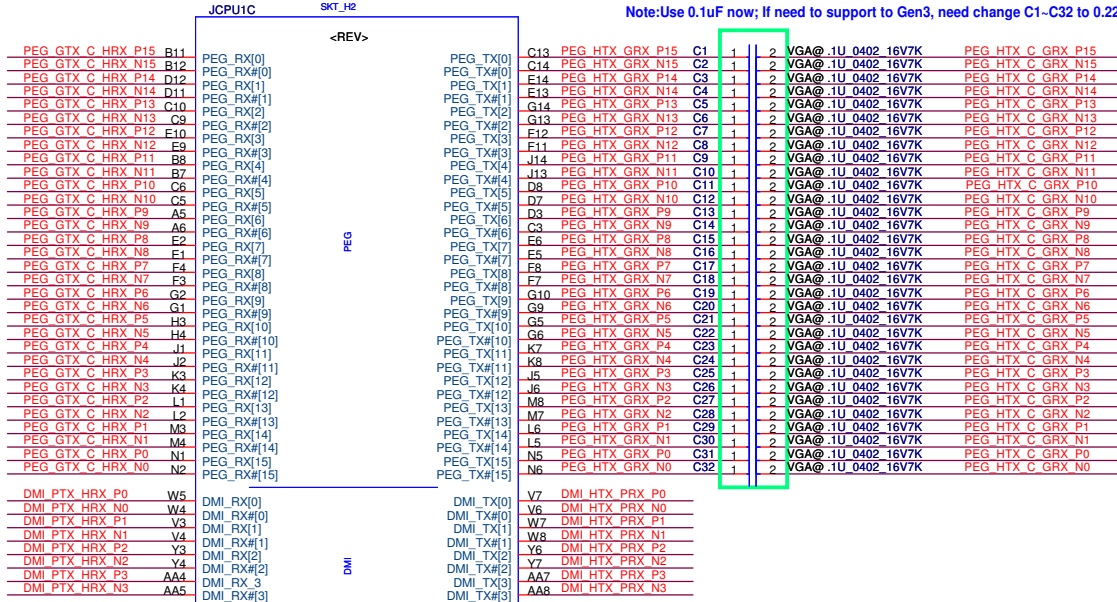
BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
TAS3208	3208@
PCML606	1606@
Samsung VRAM	X76_SAM@
Hynix VRAM	X76_HYN@
CRT	CRT@

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DMI_PTX_HRX_N[0..3] <15>
DMI_PTX_HRX_P[0..3] <15>
DMI_HTX_PRX_N[0..3] <15>
DMI_HTX_PRX_P[0..3] <15>

PEG GTX_C_HRX_P[0..15] <23>
PEG GTX_C_HRX_N[0..15] <23>
PEG HTX_C_GRX_P[0..15] <23>
PEG HTX_C_GRX_N[0..15] <23>

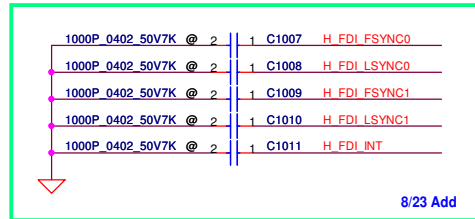
Note: Use 0.1uF now; If need to support to Gen3, need change C1-C32 to 0.22uF.



7/20 PE_RX[0-3]/PE_RX#[0-3] only use on Workstation.

7/20 PE_TX[0-3]/PE_TX#[0-3] only use on Workstation.

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)



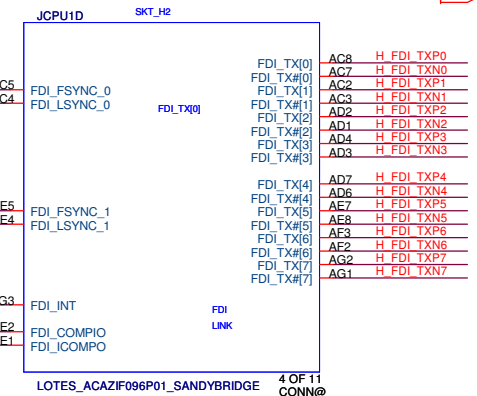
8/23 Add

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H_FDI_TXP[0..7] <17>

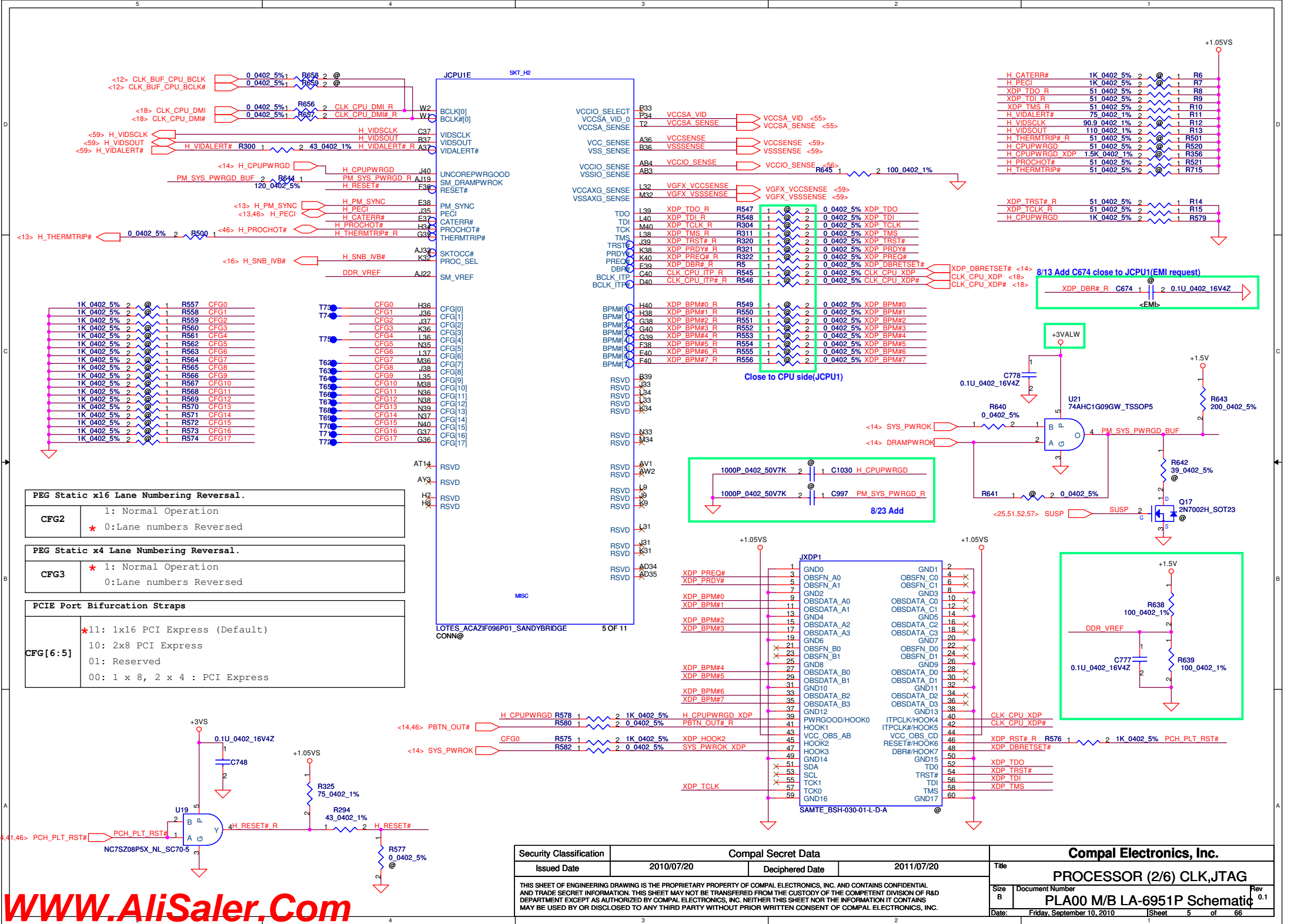
<17> H_FDI_FSYNC0
<17> H_FDI_LSYNC0

<17> H_FDI_FSYNC1
<17> H_FDI_LSYNC1

<17> H_FDI_INT
FDI_ICOMP

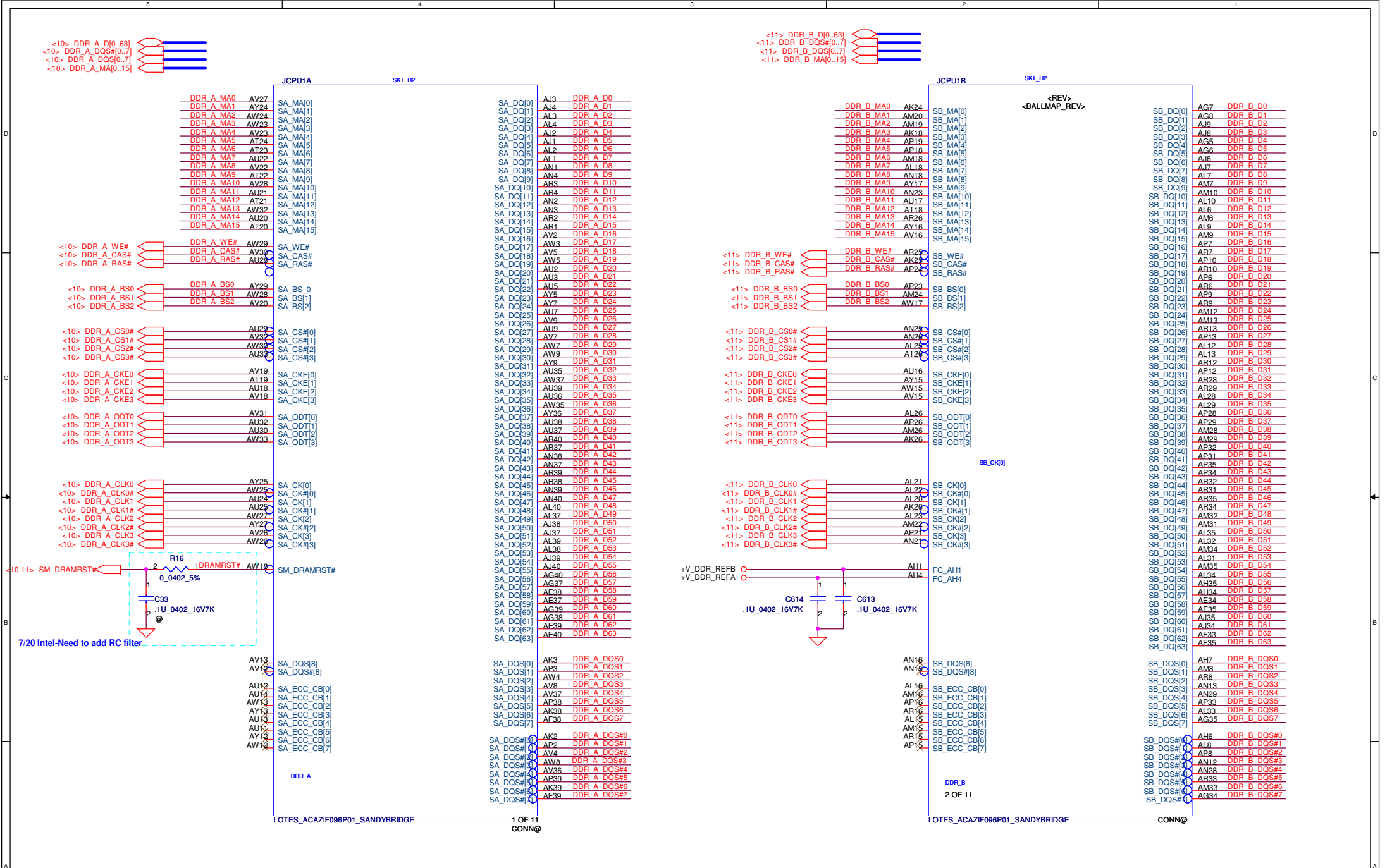


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						Size B	Document Number			Rev	
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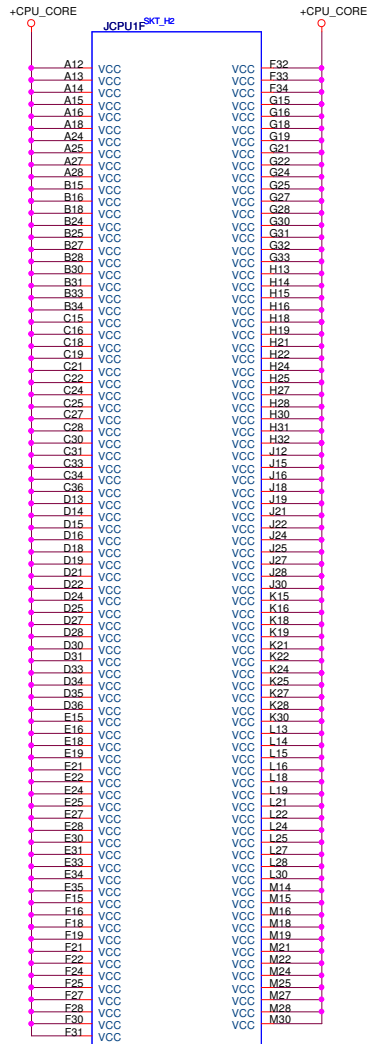
PEG Static x16 Lane Numbering Reversal.	
CFG2	1: Normal Operation ★ 0: Lane numbers Reversed
PEG Static x4 Lane Numbering Reversal.	
CFG3	★ 1: Normal Operation 0: Lane numbers Reversed
PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: 1x16 PCI Express (Default) 10: 2x8 PCI Express 01: Reserved 00: 1 x 8, 2 x 4 : PCI Express

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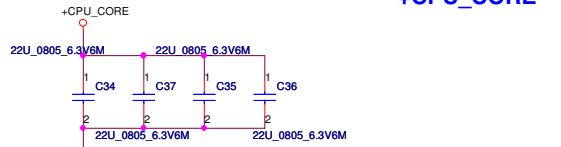
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	PROCESSOR (3/6) DDRIII	
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+CPU_CORE:112A

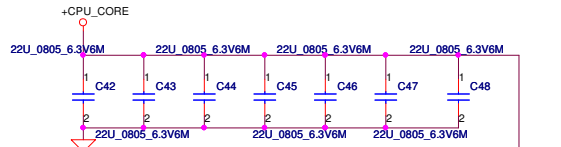


CPU POWER
6 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

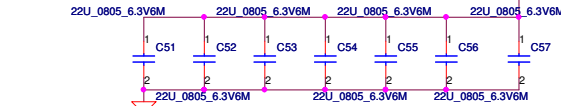
+CPU_CORE



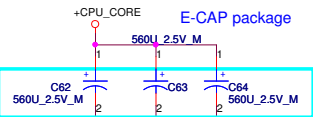
(Place these capacitors inside CPU socket cavity, top layer)



(Place these capacitors under CPU socket, Bottom layer)

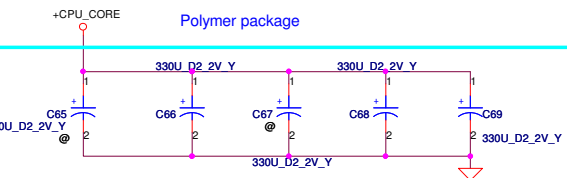


(Place these capacitors under CPU socket, Bottom layer)



8/24Change symbol of C62-C63 from SF000001P00 to SF000001K00

(Place C62-C64 capacitors under CPU socket, Top layer)

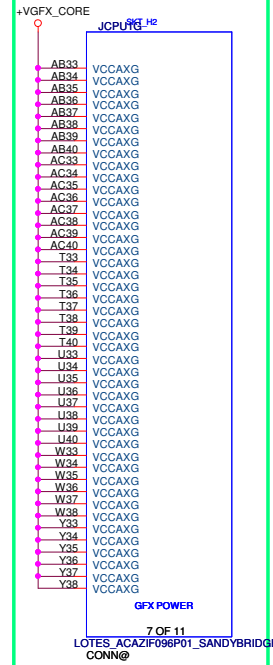


8/24Change symbol of C65-C69 from SF000002O00 to SGA20331E10

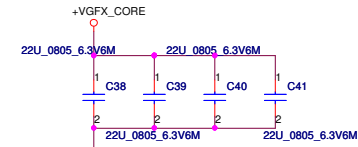
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(Place C65-C69 capacitors under CPU socket, Bottom layer)

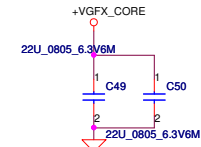
+VGFX_CORE:35A



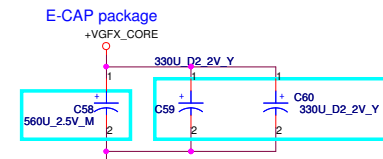
+VGFX_CORE



(Place these capacitors inside CPU socket cavity, top layer)



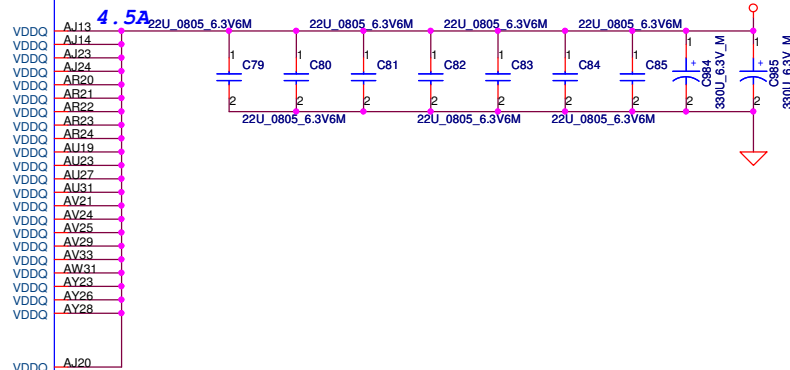
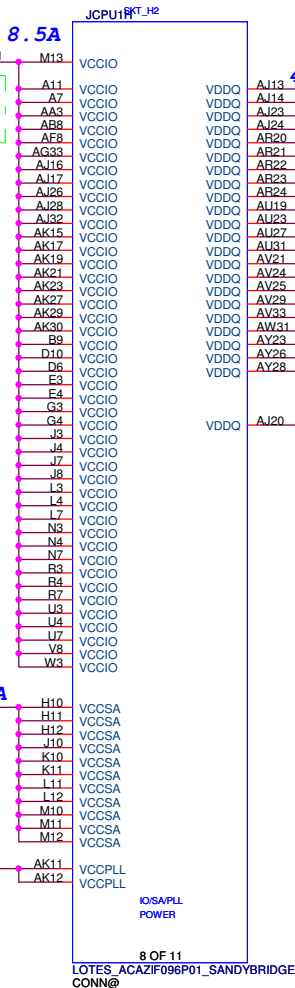
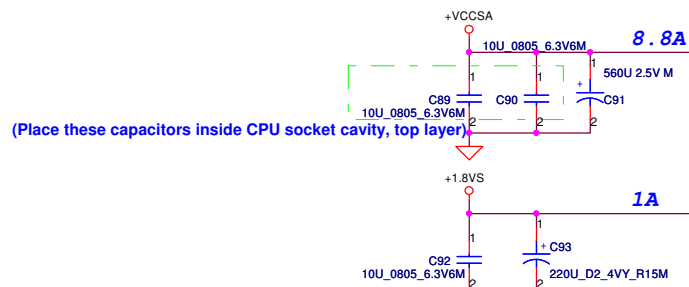
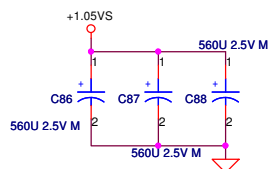
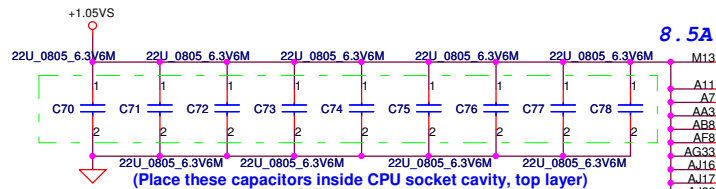
(Place these capacitors under CPU socket, Bottom layer)



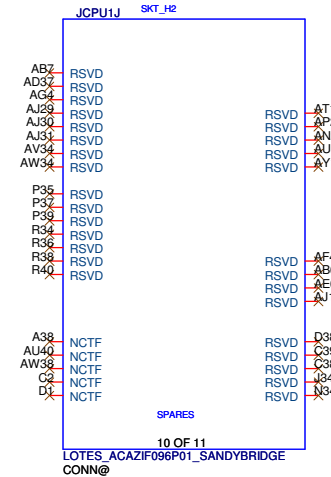
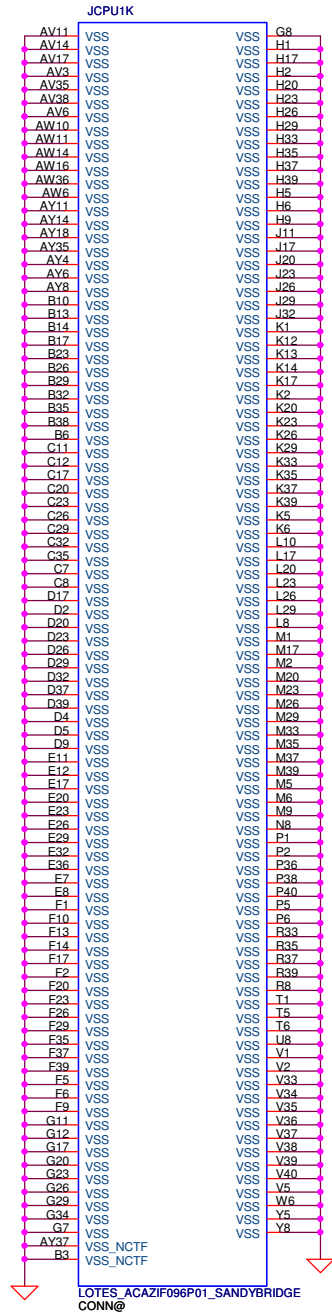
(Place C58 capacitors under CPU socket, Top layer)

(Place C59/C60 capacitors under CPU socket, Bottom layer)

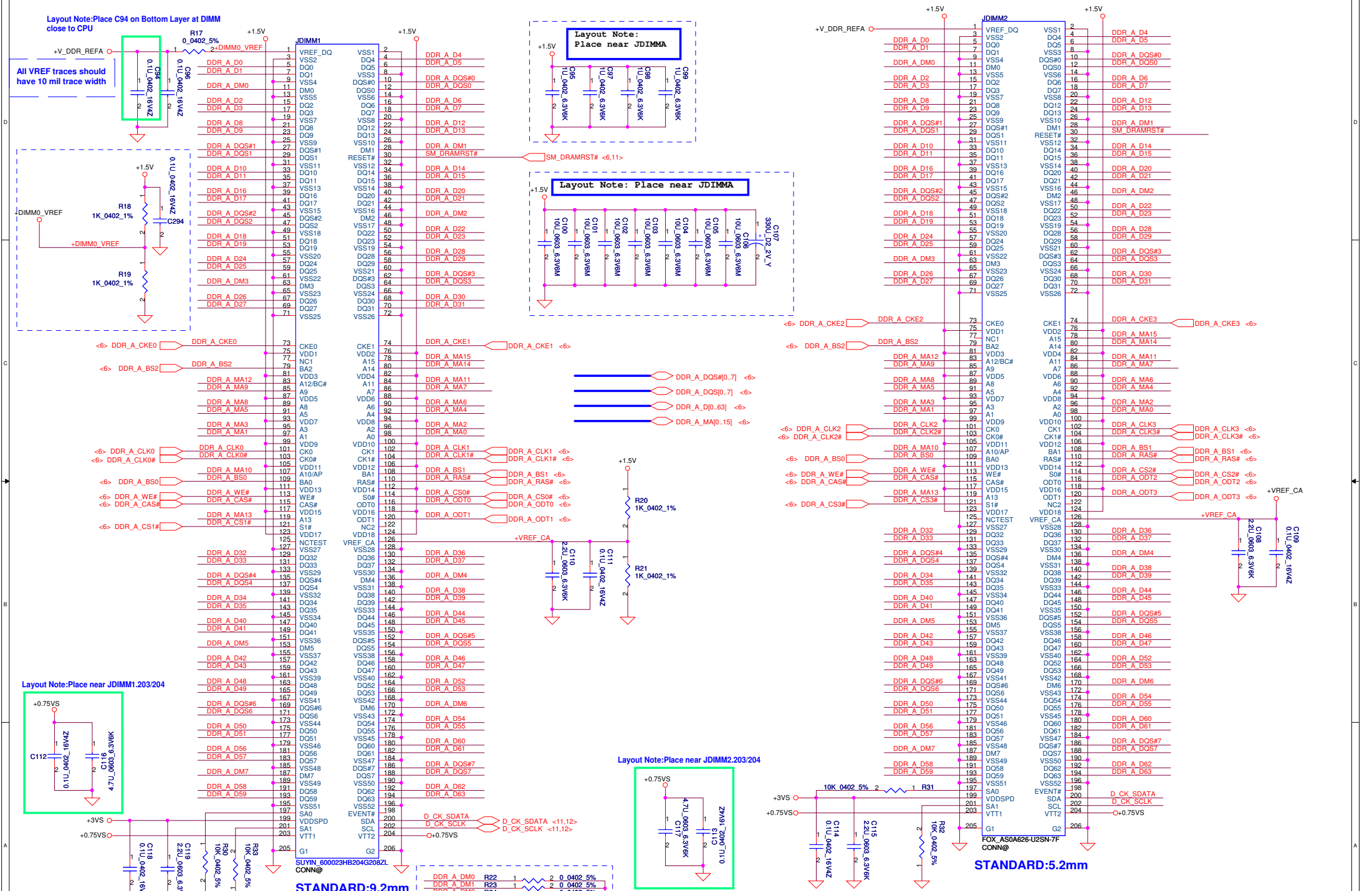
8/24Change symbol of C58 from SF000001P00 to SF000001K00
8/24Change symbol of C59/C60 from SF000001P00 to SGA20331E10



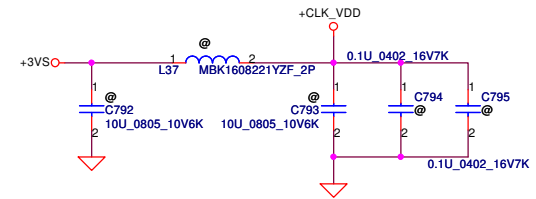
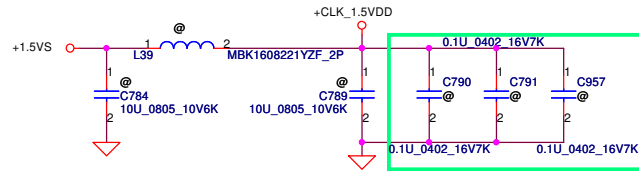
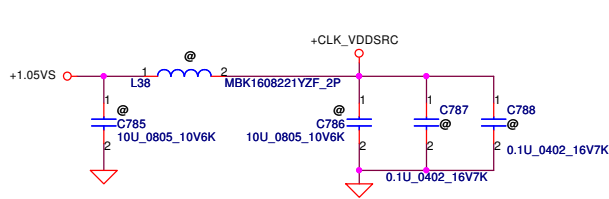
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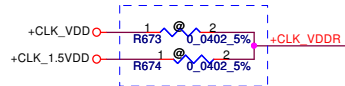
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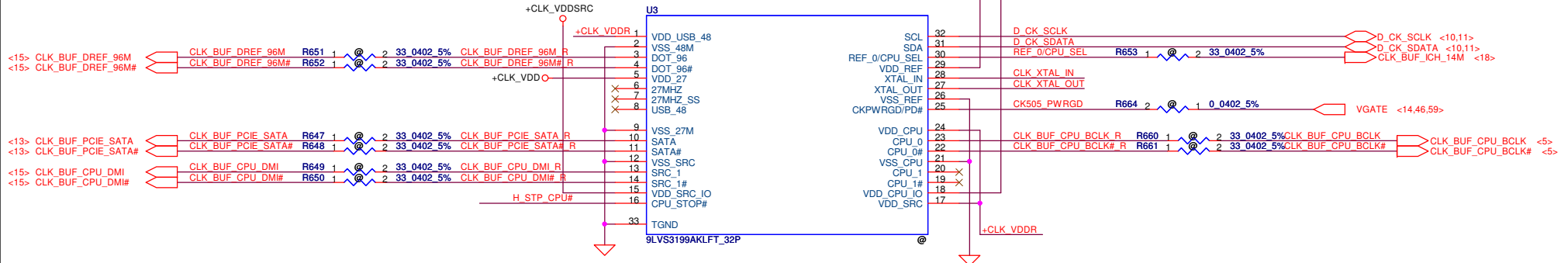




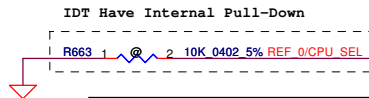
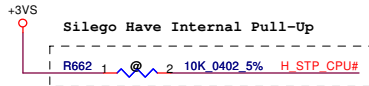
Layout Note: Close C790/C791/C957 close to U3.Pin1.17.24



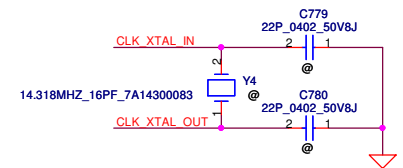
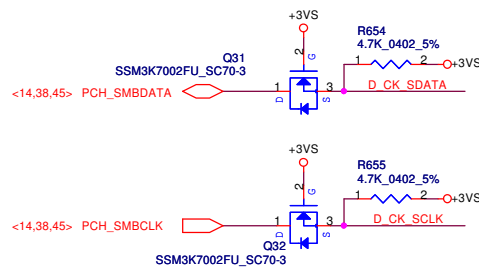
Clock Generator



LOW Power:
Realtek: RIM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00

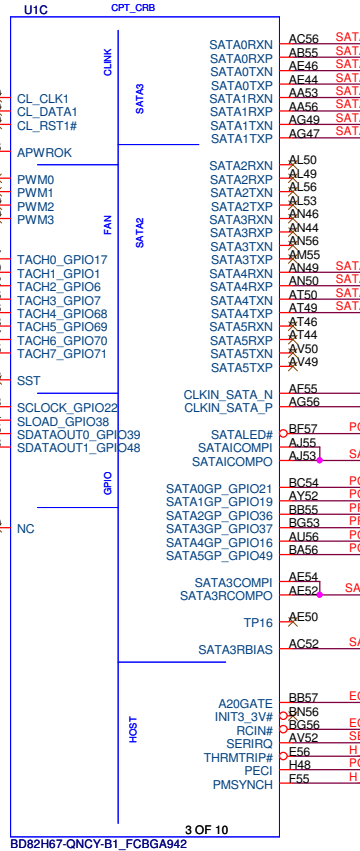
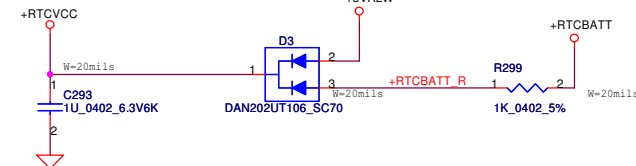
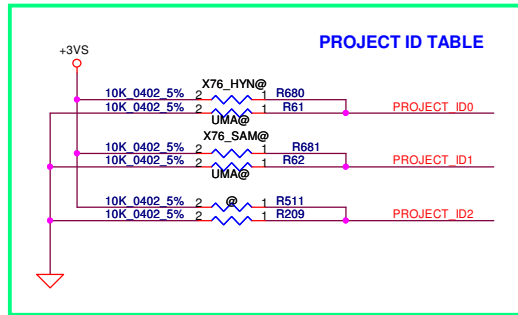
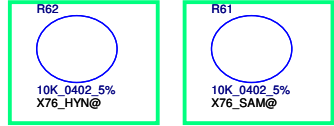


PIN	30	CPU_0	CPU_1
0 (Default)		133MHz	133MHz
1		100MHz	100MHz

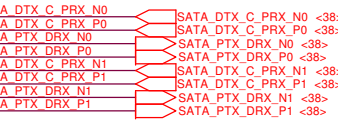


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Size	Document Number	Rev		0.1	
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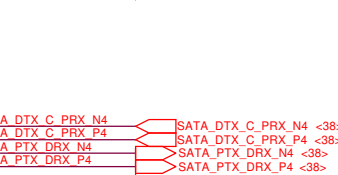
9/8 Add



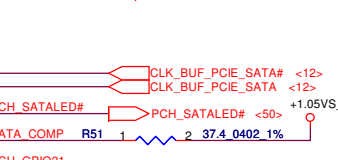
BD82H67-QNCY-B1_FCBGA942



SATA for SSD



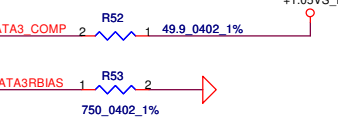
SATA for HDD



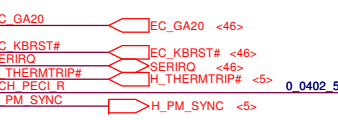
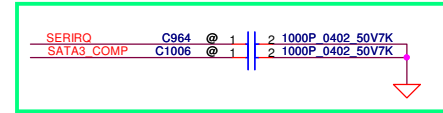
SATA for ODD



Boot BIOS Strap Bit 0 (GPIO19)

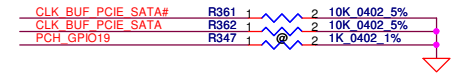
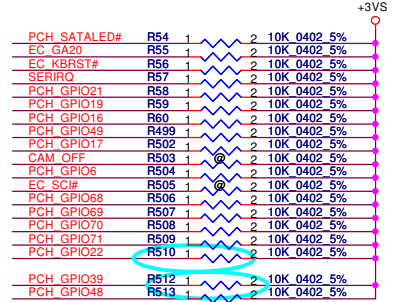


Layout Note: SATA_COMP WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.



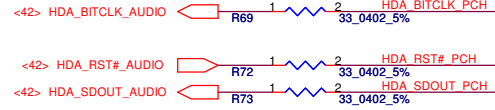
7/30 R510--- CRB:1K ohm;EDS:10K ohm

7/30 R512--- CRB:10K ohm PD to GND;EDS:10K ohm PU to +3VS



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				Size Custom	Document Number	Rev 0.1
				PLA00 M/B LA-6951P Schematic		
				Date:	Friday, September 10, 2010	Sheet 13 of 66

HDA for AUDIO

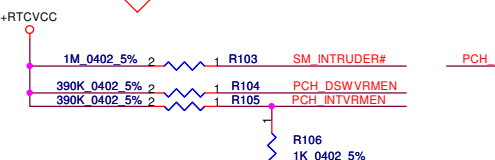
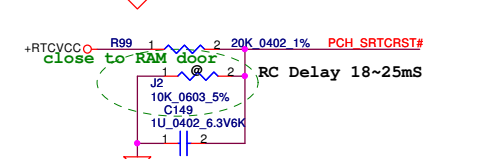
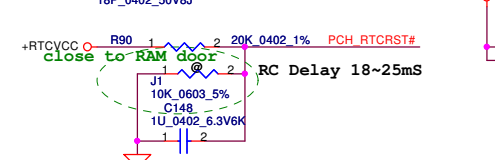
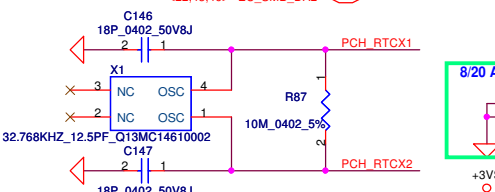
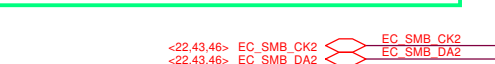
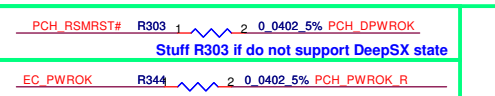
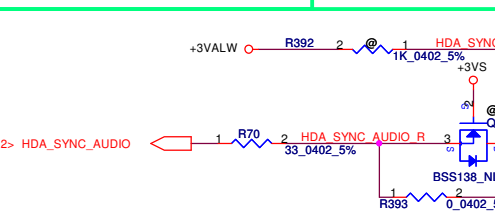


HDA_SDO

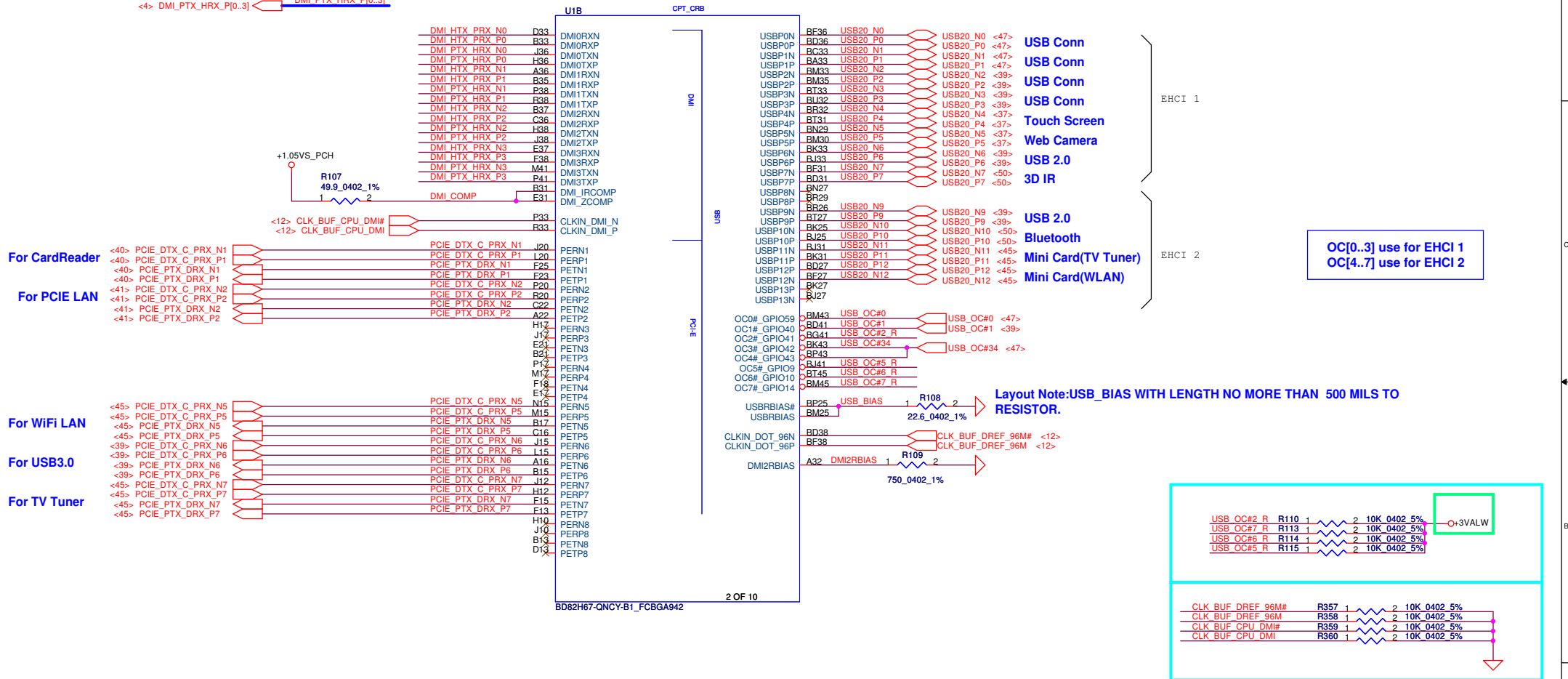
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC

This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
★L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

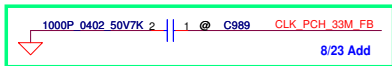
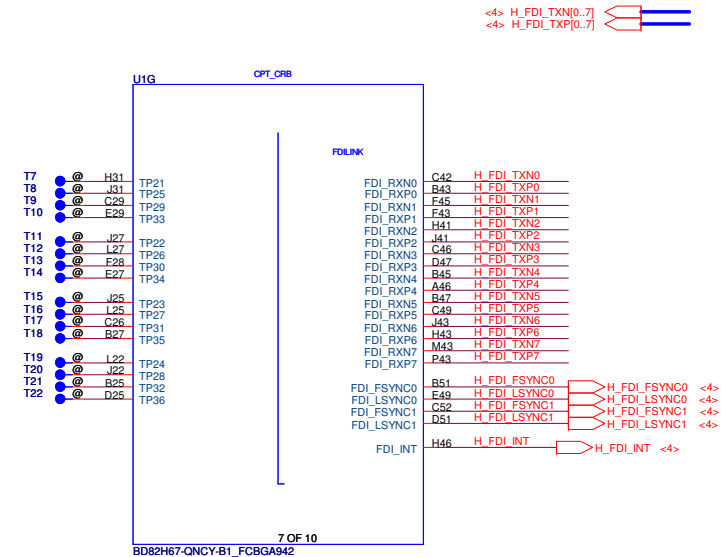
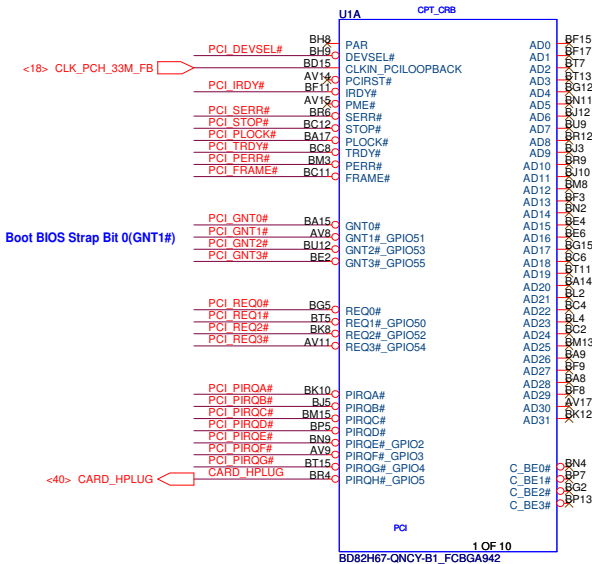
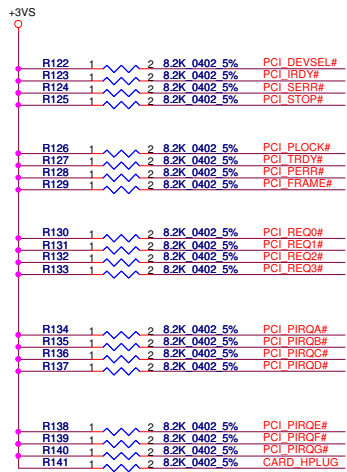


<4> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
<4> DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
<4> DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
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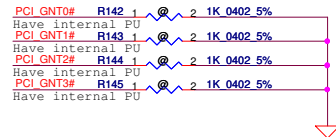


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						Size A	Document Number			Rev 0.1	
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						Date:		Friday, September 10, 2010		Sheet 15 of 66	



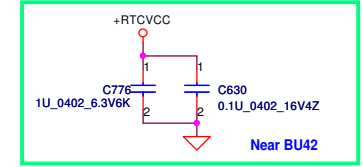
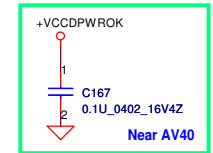
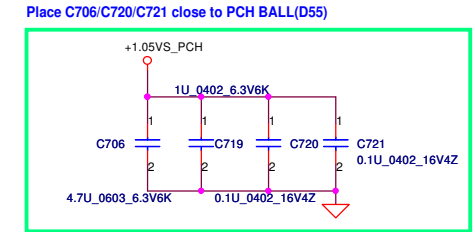
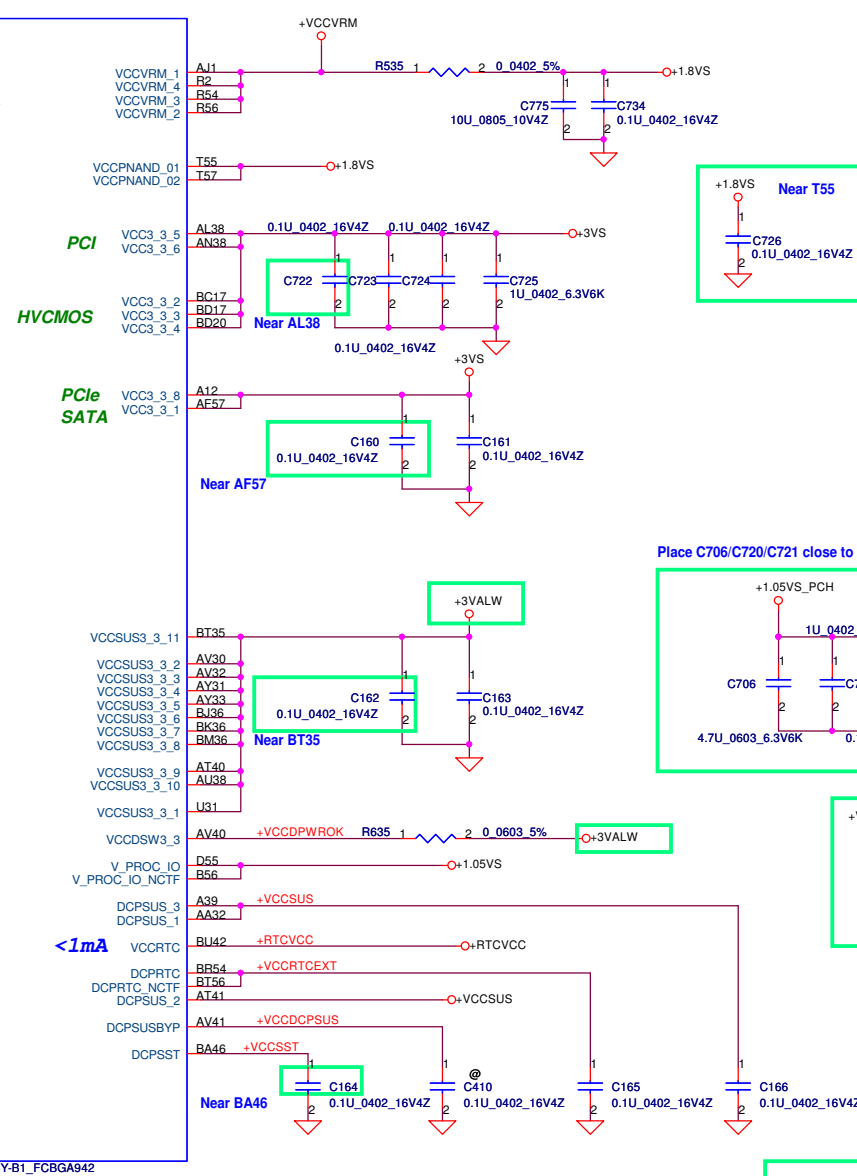
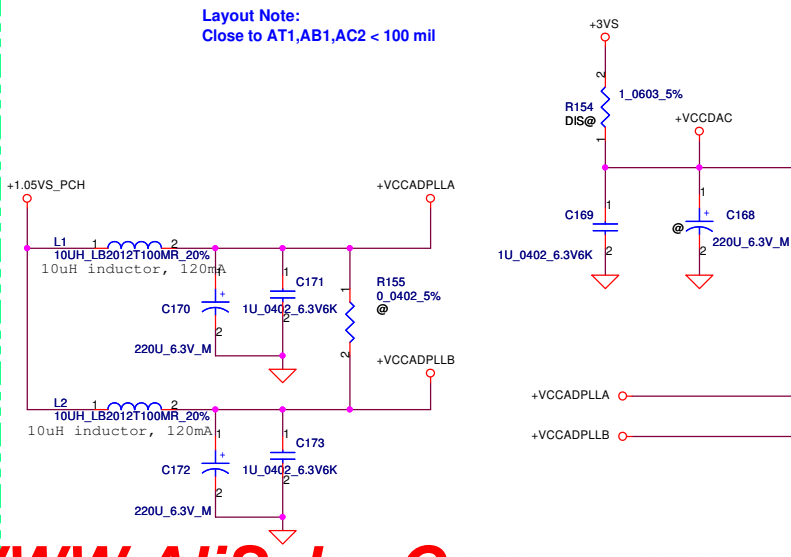
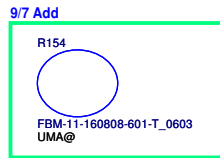
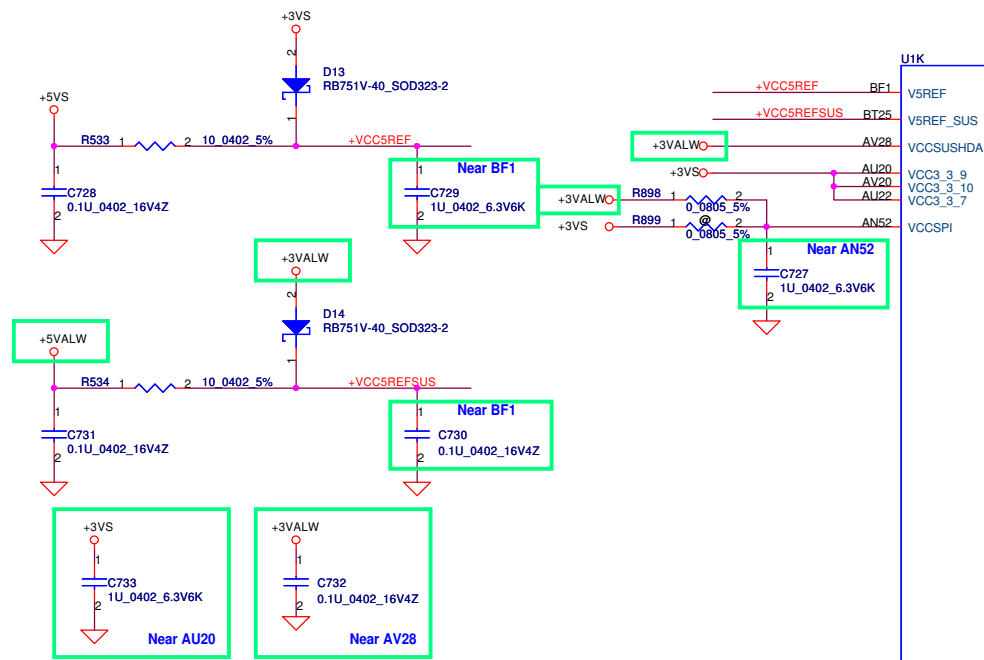


Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★



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OPT_C08		
BC15	VSS_125	VSS_5
BC20	VSS_126	VSS_6
BC27	VSS_127	VSS_7
BC31	VSS_128	VSS_8
BC38	VSS_129	VSS_9
BC47	VSS_130	VSS_10
BC9	VSS_131	VSS_11
BD25	VSS_132	VSS_12
BD33	VSS_133	VSS_13
BF12	VSS_134	VSS_14
BF20	VSS_135	VSS_15
BF25	VSS_136	VSS_16
BF33	VSS_137	VSS_17
BF41	VSS_138	VSS_18
BF43	VSS_139	VSS_19
BF46	VSS_140	VSS_20
BF52	VSS_141	VSS_21
BF6	VSS_142	VSS_22
BG22	VSS_143	VSS_23
BG25	VSS_144	VSS_24
BG27	VSS_145	VSS_25
BG31	VSS_146	VSS_26
BG33	VSS_147	VSS_27
BG36	VSS_148	VSS_28
BG38	VSS_149	VSS_29
BH52	VSS_150	VSS_30
BH6	VSS_151	VSS_31
BH6	VSS_152	VSS_32
BJ1	VSS_153	VSS_33
BJ15	VSS_154	VSS_34
BK20	VSS_155	VSS_35
BK41	VSS_156	VSS_36
BK52	VSS_157	VSS_37
BK6	VSS_158	VSS_38
BM10	VSS_159	VSS_39
BM12	VSS_160	VSS_40
BM16	VSS_161	VSS_41
BM22	VSS_162	VSS_42
BM23	VSS_163	VSS_43
BM26	VSS_164	VSS_44
BM28	VSS_165	VSS_45
BM32	VSS_166	VSS_46
BM40	VSS_167	VSS_47
BM45	VSS_168	VSS_48
BM48	VSS_169	VSS_49
BM5	VSS_170	VSS_50
BM31	VSS_171	VSS_51
BM47	VSS_172	VSS_52
BN6	VSS_173	VSS_53
BP3	VSS_174	VSS_54
BP33	VSS_175	VSS_55
BP35	VSS_176	VSS_56
BR22	VSS_177	VSS_57
BR52	VSS_178	VSS_58
BU19	VSS_179	VSS_59
BU26	VSS_180	VSS_60
BU29	VSS_181	VSS_61
BU36	VSS_182	VSS_62
BU39	VSS_183	VSS_63
C19	VSS_184	VSS_64
C32	VSS_185	VSS_65
C39	VSS_186	VSS_66
C4	VSS_187	VSS_67
D23	VSS_188	VSS_68
D3	VSS_189	VSS_69
D35	VSS_190	VSS_70
D45	VSS_191	VSS_71
D45	VSS_192	VSS_72
E19	VSS_193	VSS_73
E39	VSS_194	VSS_74
E54	VSS_195	VSS_75
E6	VSS_196	VSS_76
E9	VSS_197	VSS_77
F10	VSS_198	VSS_78
F12	VSS_199	VSS_79
F18	VSS_200	VSS_80
F22	VSS_201	VSS_81
F26	VSS_202	VSS_82
F32	VSS_203	VSS_83
F33	VSS_204	VSS_84
F35	VSS_205	VSS_85
F38	VSS_206	VSS_86
F40	VSS_207	VSS_87
F42	VSS_208	VSS_88
F46	VSS_209	VSS_89
F48	VSS_210	VSS_90
F50	VSS_211	VSS_91
F8	VSS_212	VSS_92
AV18	VSS_213	VSS_93
AV22	VSS_104	VSS_94
AV34	VSS_105	VSS_95
AV38	VSS_106	VSS_96
AV47	VSS_107	VSS_97
AV6	VSS_108	VSS_98
AW57	VSS_109	VSS_99
AY38	VSS_110	VSS_100
AY6	VSS_111	VSS_101
B23	VSS_112	VSS_102
BA11	VSS_113	VSS_103
BA12	VSS_114	VSS_104
BA31	VSS_115	VSS_105
BA41	VSS_116	VSS_106
BA44	VSS_117	VSS_107
GA54	VSS_118	VSS_108
H15	VSS_119	VSS_109
H20	VSS_120	VSS_110
H22	VSS_121	VSS_111
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H27	VSS_123	VSS_113
H33	VSS_124	VSS_114
H6	VSS_125	VSS_115
J1	VSS_126	VSS_116
J33	VSS_127	VSS_117
J46	VSS_128	VSS_118
J48	VSS_129	VSS_119
J5	VSS_130	VSS_120
J53	VSS_131	VSS_121
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K6	VSS_133	VSS_123
K9	VSS_134	VSS_124
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	VSS_258	VSS_248
	VSS_259	VSS_249

U1L		
L12	VSS_231	TP3
L17	VSS_232	TP13
L38	VSS_233	TP17
L41	VSS_234	TP18
L43	VSS_235	TP19
M20	VSS_236	TP20
M22	VSS_237	TP1
M25	VSS_238	TP4
M27	VSS_239	VSS_296
M31	VSS_240	VSS_295
T52	VSS_241	VSS_294
T6	VSS_242	VSS_293
U11	VSS_262	TP2
U17	VSS_263	TP5
U20	VSS_264	VSS_292
U22	VSS_265	VSS_291
U25	VSS_266	
U27	VSS_267	
U33	VSS_268	TP14
U36	VSS_269	TP15
U38	VSS_270	TP11
U41	VSS_271	
U47	VSS_272	
U53	VSS_273	
U53	VSS_274	
U53	VSS_275	
U53	VSS_276	
U53	VSS_277	
U53	VSS_278	
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U53	VSS_285	
U53	VSS_286	
U53	VSS_287	
U53	VSS_288	
U53	VSS_289	
U53	VSS_290	
A4	VSS_NCTF_1	
A6	VSS_NCTF_2	
AK52	VSS_NCTF_3	
BM1	VSS_NCTF_4	
BM57	VSS_NCTF_5	
BP1	VSS_NCTF_6	
BT2	VSS_NCTF_7	
BU4	VSS_NCTF_8	
BU52	VSS_NCTF_9	
BU54	VSS_NCTF_10	
D1	VSS_NCTF_11	
D1	VSS_NCTF_12	
F1	VSS_NCTF_13	
F1	VSS_NCTF_14	
AY22	VSS_4	
C12	VSS_3	
AE56	VSS_1	
BR36	VSS_2	
AU2	VSSADAC	
A54	TS_VSS1	
A52	TS_VSS2	
F57	TS_VSS3	
D57	TS_VSS4	

NOTE: PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLCTEN and L_BKLCTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

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								Size	Document Number	Rev
								Custom	PLA00 M/B LA-6951P Schematic	0.1
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To HDMI-out

To 2D/3D Vision

To 3D Vision

HDMI-OUT

Scalar

Part 4 of 7

NC

LVDS/TMDS

TEST

SERIAL

GENERAL

External VGA Thermal Sensor

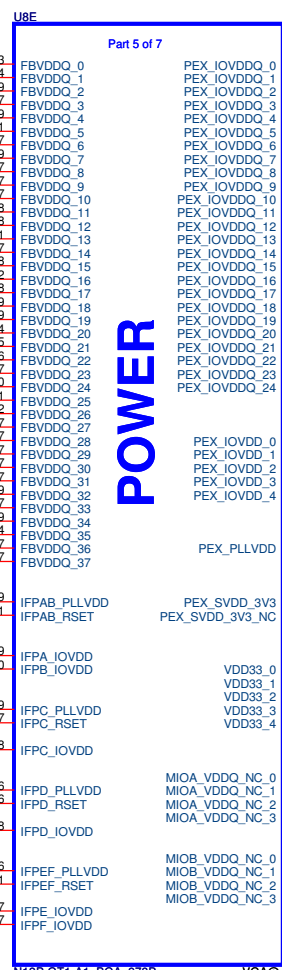
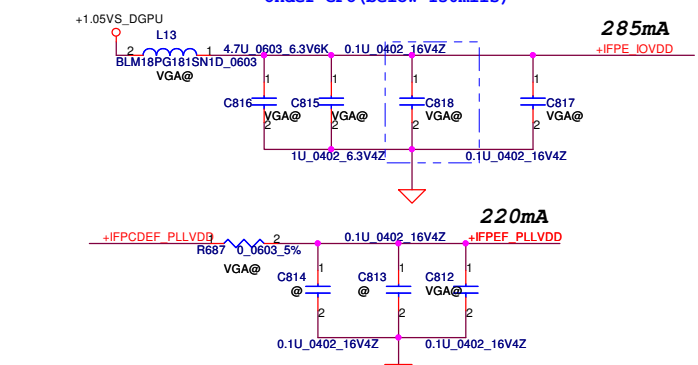
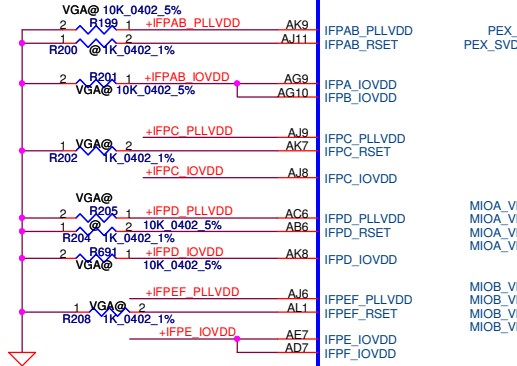
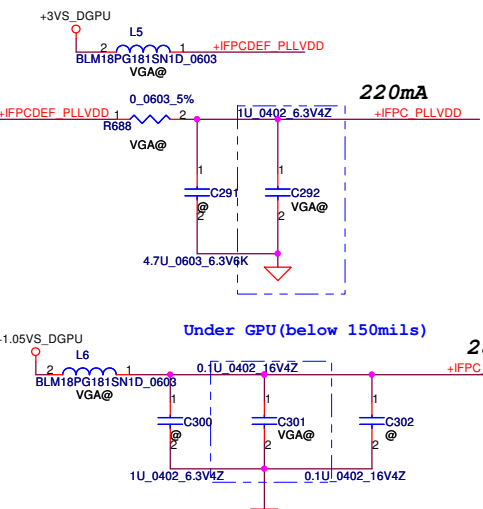
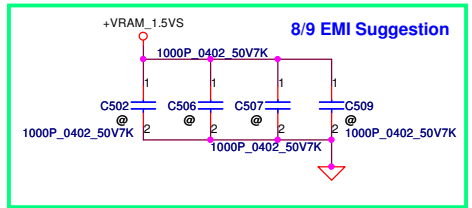
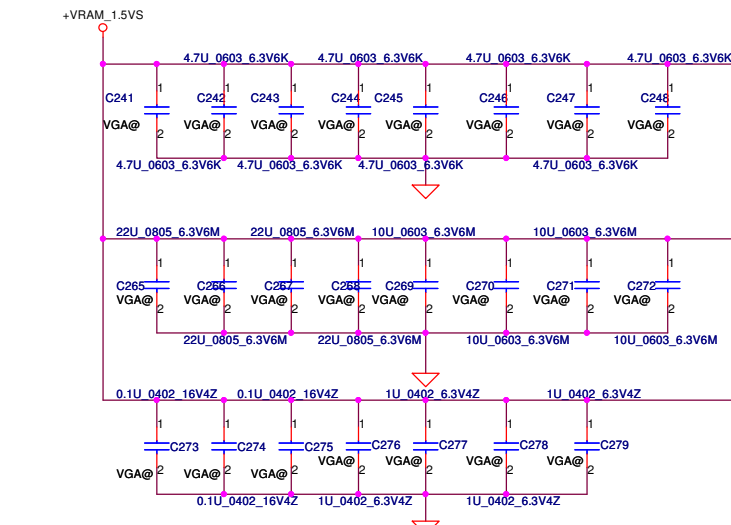
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Internal Thermal Sensor

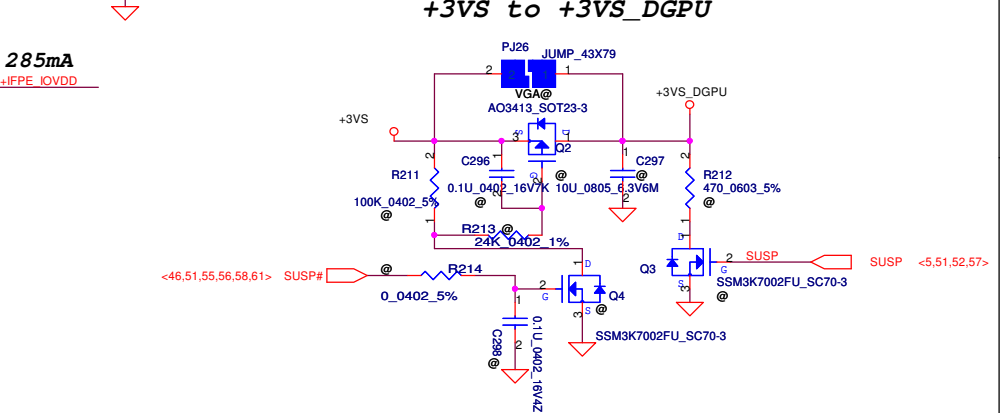
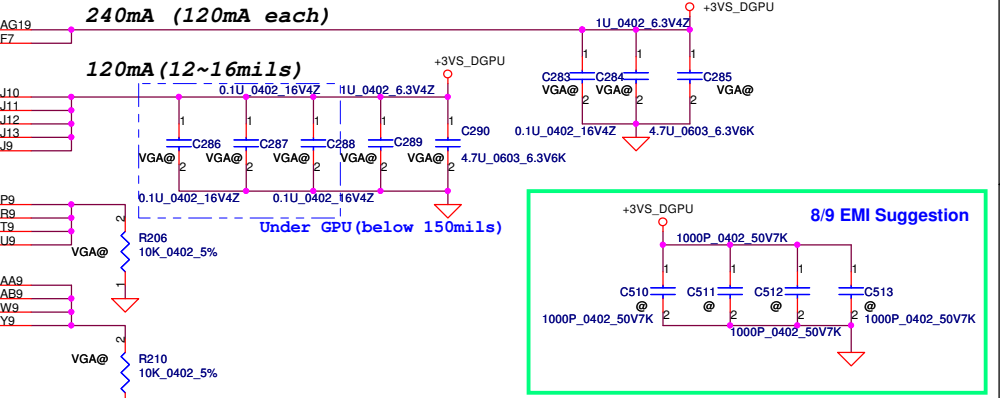
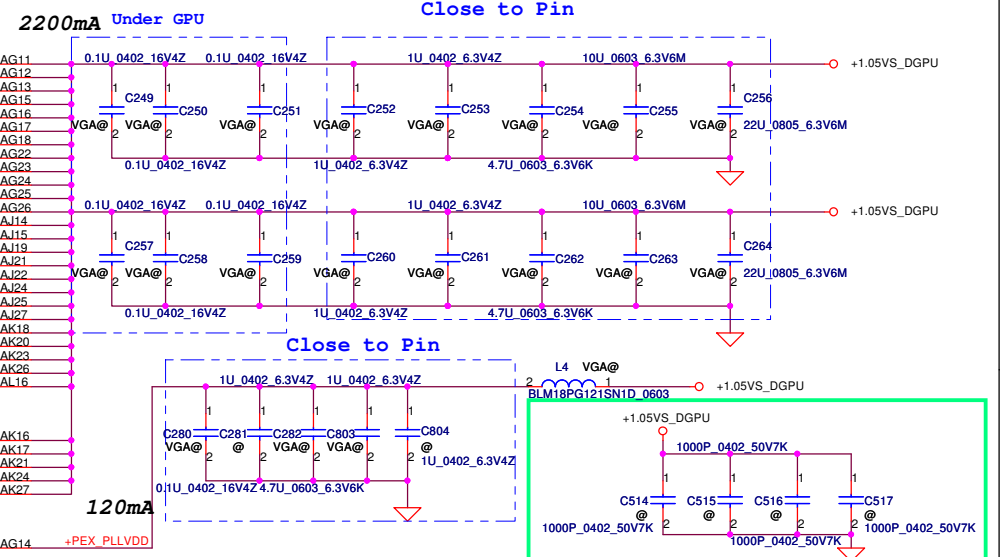
Address: 0x9E H

Reserve VBIOS for NV suggest (1Mbit)

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					VGA(1/12)-LVDS/HDMI/DP/THM				
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					PLA00 M/B LA-6951P Schematic	0.1			
				Date:	Friday, September 10, 2010	Sheet	22	of	66

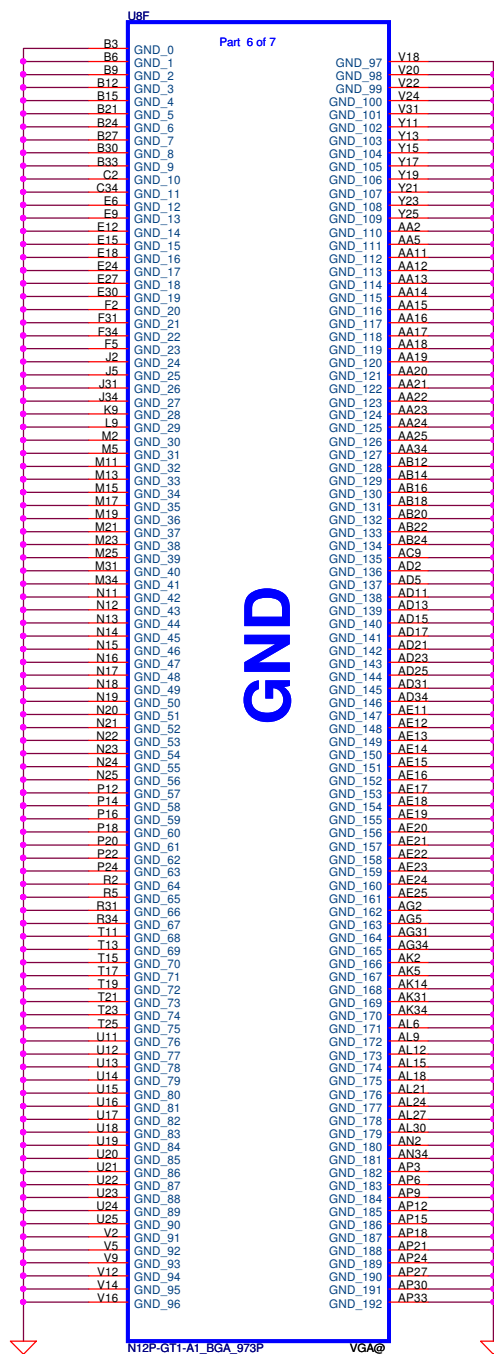


POWER



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Date	Friday, September 10, 2010	Sheet	25	of 66	

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								PLA00 M/B LA-6951P Schematic		0.1	
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<31,32> MDB[0..63] ← MDB[0..63]

MDB0 B13 FBC_D0
MDB1 D13 FBC_D1
MDB2 A13 FBC_D2
MDB3 C16 FBC_D3
MDB4 C16 FBC_D4
MDB5 B16 FBC_D5
MDB6 A17 FBC_D6
MDB7 D16 FBC_D7
MDB8 C13 FBC_D8
MDB9 B11 FBC_D9
MDB10 C11 FBC_D10
MDB11 A11 FBC_D11
MDB12 C10 FBC_D12
MDB13 B8 FBC_D13
MDB14 A8 FBC_D14
MDB15 E8 FBC_D15
MDB16 F8 FBC_D16
MDB17 F12 FBC_D17
MDB18 F10 FBC_D18
MDB19 F9 FBC_D19
MDB20 E12 FBC_D20
MDB21 D8 FBC_D21
MDB22 D11 FBC_D22
MDB23 E11 FBC_D23
MDB24 D12 FBC_D24
MDB25 E13 FBC_D25
MDB26 F13 FBC_D26
MDB27 F14 FBC_D27
MDB28 E15 FBC_D28
MDB29 F16 FBC_D29
MDB30 F16 FBC_D30
MDB31 F17 FBC_D31
MDB32 D29 FBC_D32
MDB33 E27 FBC_D33
MDB34 F28 FBC_D34
MDB35 E28 FBC_D35
MDB36 D26 FBC_D36
MDB37 F25 FBC_D37
MDB38 D24 FBC_D38
MDB39 E25 FBC_D39
MDB40 E32 FBC_D40
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MDB43 E31 FBC_D43
MDB44 C33 FBC_D44
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MDB46 D30 FBC_D46
MDB47 E29 FBC_D47
MDB48 B29 FBC_D48
MDB49 C31 FBC_D49
MDB50 C29 FBC_D50
MDB51 B31 FBC_D51
MDB52 C32 FBC_D52
MDB53 B32 FBC_D53
MDB54 B35 FBC_D54
MDB55 B34 FBC_D55
MDB56 A29 FBC_D56
MDB57 B28 FBC_D57
MDB58 A28 FBC_D58
MDB59 C26 FBC_D59
MDB60 D25 FBC_D60
MDB61 B25 FBC_D61
MDB62 FBC_D62
MDB63 A25 FBC_D63

Part 3 of 7

MEMORY INTERFACE C

FBC_CMD0 E18 CMDB0
FBC_CMD1 E19 CMDB1
FBC_CMD2 D19 CMDB2
FBC_CMD3 G17 CMDB3
FBC_CMD4 F19 CMDB4
FBC_CMD5 C19 CMDB5
FBC_CMD6 B17 CMDB6
FBC_CMD7 E20 CMDB7
FBC_CMD8 B19 CMDB8
FBC_CMD9 D20 CMDB9
FBC_CMD10 A19 CMDB10
FBC_CMD11 D19 CMDB11
FBC_CMD12 C20 CMDB12
FBC_CMD13 F20 CMDB13
FBC_CMD14 B20 CMDB14
FBC_CMD15 G21 CMDB15
FBC_CMD16 F22 CMDB16
FBC_CMD17 F24 CMDB17
FBC_CMD18 E23 CMDB18
FBC_CMD19 C25 CMDB19
FBC_CMD20 C23 CMDB20
FBC_CMD21 E22 CMDB21
FBC_CMD22 D21 CMDB22
FBC_CMD23 A23 CMDB23
FBC_CMD24 D22 CMDB24
FBC_CMD25 B22 CMDB25
FBC_CMD26 B23 CMDB26
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FBC_CMD28 B22 CMDB28
FBC_CMD29 A22 CMDB29
FBC_CMD30 A20 CMDB30
FBC_CMD31 G20 X

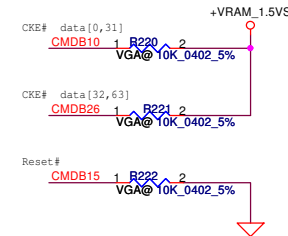
FBC_DOM0 A16 DOMB0
FBC_DOM1 D10 DOMB1
FBC_DOM2 D15 DOMB2
FBC_DOM3 D27 DOMB3
FBC_DOM4 D34 DOMB4
FBC_DOM5 A34 DOMB5
FBC_DOM6 D28 DOMB6
FBC_DOM7

FBC_DQS_RN0 B14 T43 @
FBC_DQS_RN1 B10 T44 @
FBC_DQS_RN2 D9 T45 @
FBC_DQS_RN3 E14 T46 @
FBC_DQS_RN4 F26 T47 @
FBC_DQS_RN5 A31 T48 @
FBC_DQS_RN6 A26 T49 @
FBC_DQS_RN7

FBC_DQS_WP0 C14 DQSB0
FBC_DQS_WP1 A10 DQSB1
FBC_DQS_WP2 E10 DQSB2
FBC_DQS_WP3 D14 DQSB3
FBC_DQS_WP4 E26 DQSB4
FBC_DQS_WP5 D32 DQSB5
FBC_DQS_WP6 A32 DQSB6
FBC_DQS_WP7 B26 DQSB7

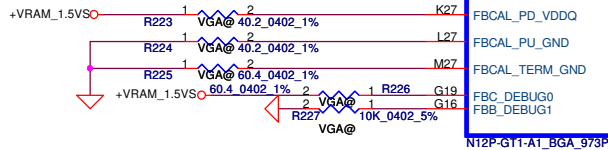
FBC_WCK0 G14 FBB_WCK01# FBB_WCK01 <31>
FBC_WCK0_N G15 FBB_WCK01# FBB_WCK01# <31>
FBC_WCK1 G11 FBB_WCK23 FBB_WCK23 <31>
FBC_WCK1_N G12 FBB_WCK23# FBB_WCK23# <31>
FBC_WCK2 G27 FBB_WCK45 FBB_WCK45 <32>
FBC_WCK2_N G28 FBB_WCK45# FBB_WCK45# <32>
FBC_WCK3 G24 FBB_WCK67 FBB_WCK67 <32>
FBC_WCK3_N G25 FBB_WCK67# FBB_WCK67# <32>

FBC_CLK0 E17 CLKB0
FBC_CLK0_N D17 CLKB0#
FBC_CLK1 D23 CLKB1
FBC_CLK1_N E23 CLKB1#



DOMB[7..0] <31,32>

DQSB[7..0] <31,32>

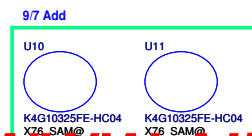
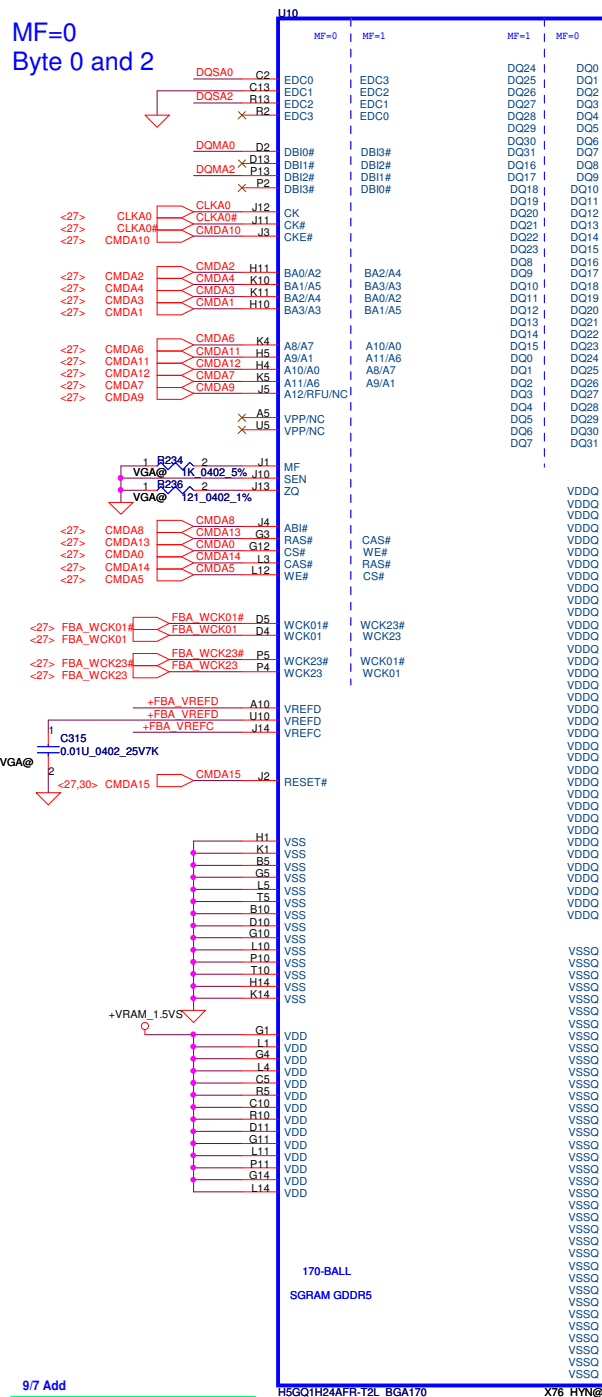


N12P-GY1-A1_BGA_973P

Mode G- Mapping

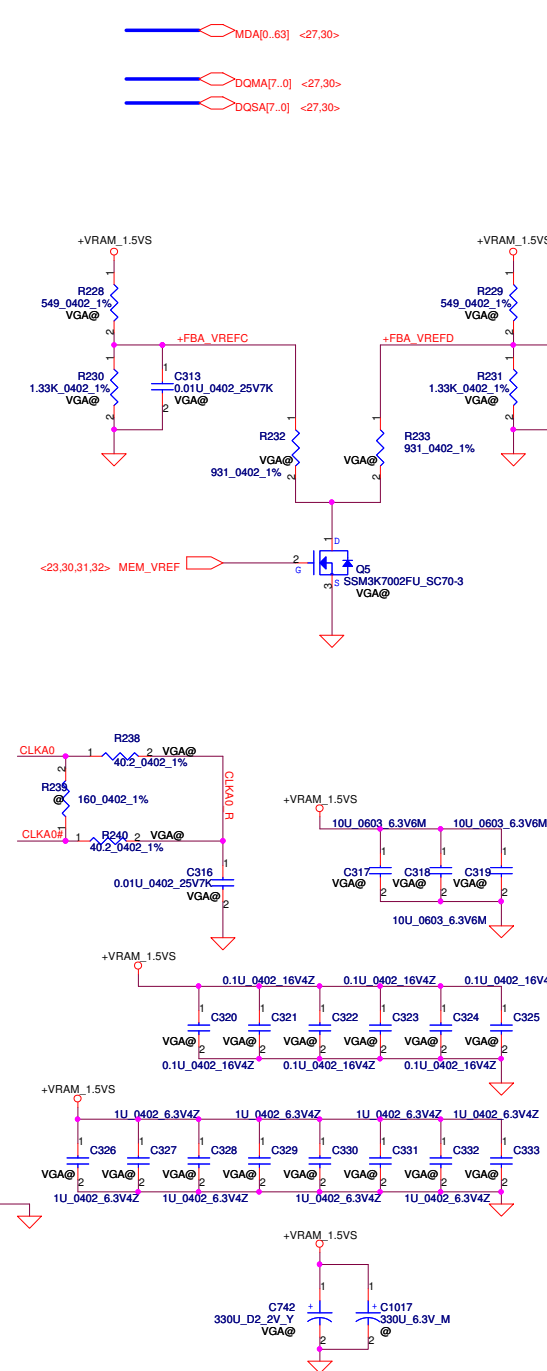
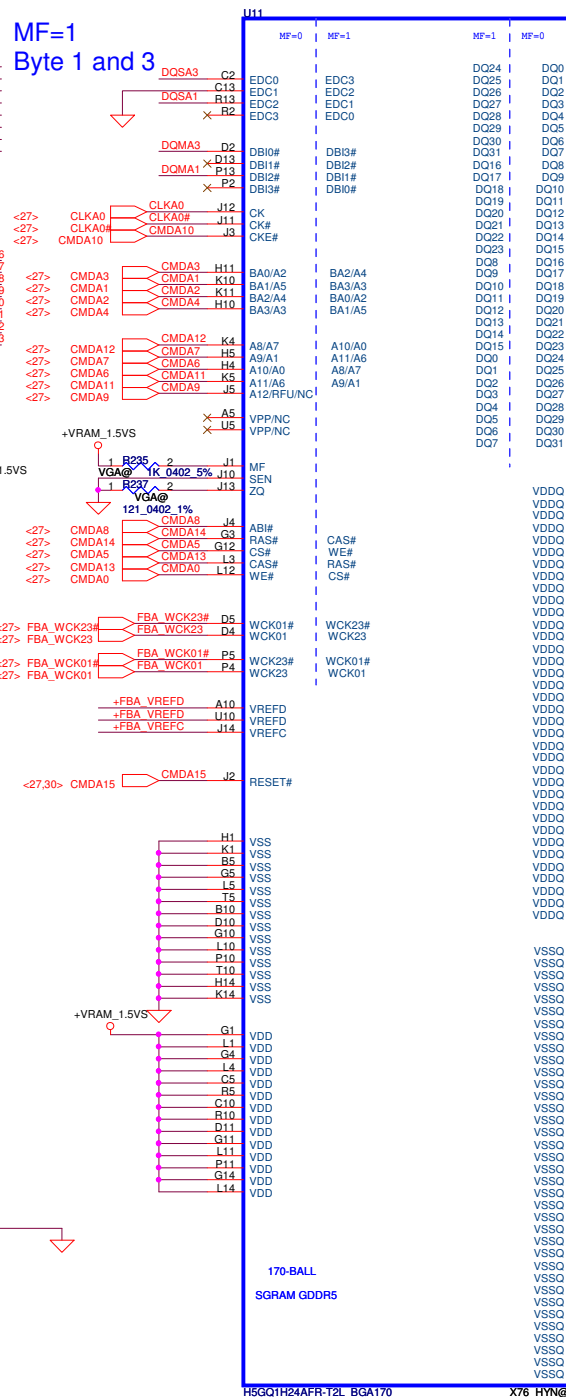
DATA Bus	
Address	0..31 32..63
CMD3	A4_BA2
CMD8	ABI#
CMD2	A2_BA0
CMD7	A6_A11
CMD15	RESET#
CMD13	RAS#
CMD4	A5_BA1
CMD6	A7_A8
CMD12	A0_A10
CMD10	CMD#
CMD9	A12_RFU
CMD1	A3_BA3
CMD11	A1_A9
CMD0	CS#
CMD5	WE#
CMD14	CAS#
CMD30	RAS#
CMD20	A3_BA3
CMD16	WE#
CMD25	A12_RFU
CMD28	A7_A8
CMD22	A0_A10
CMD19	A2_BA0
CMD17	A5_BA1
CMD27	A6_A11
CMD29	CAS#
CMD18	A4_BA2
CMD15	RESET#
CMD26	CKE#
CMD23	A1_A9
CMD24	ABI#
CMD21	CS#

MF=0
Byte 0 and 2

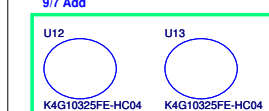


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MF=1
Byte 1 and 3



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				Custom Document Number PLA00 M/B LA-6951P Schematic	0.1
Date:		Friday, September 10, 2010		ISheet	29 of 66

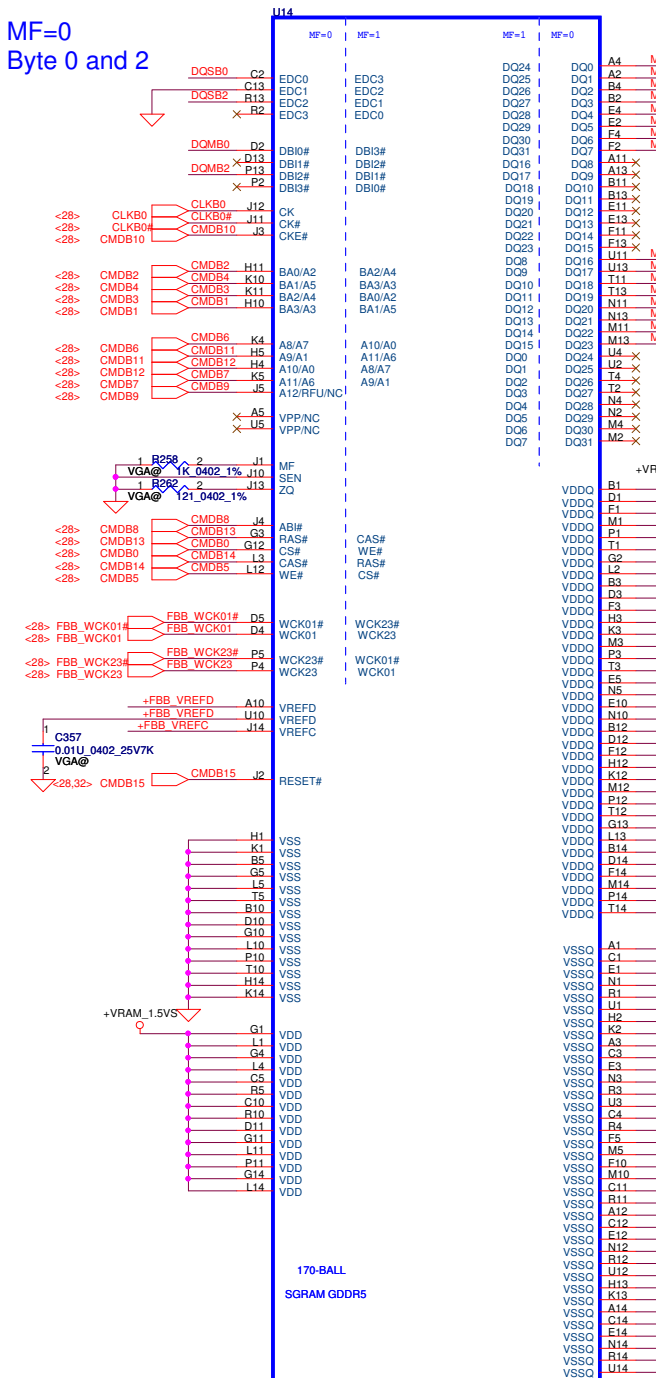


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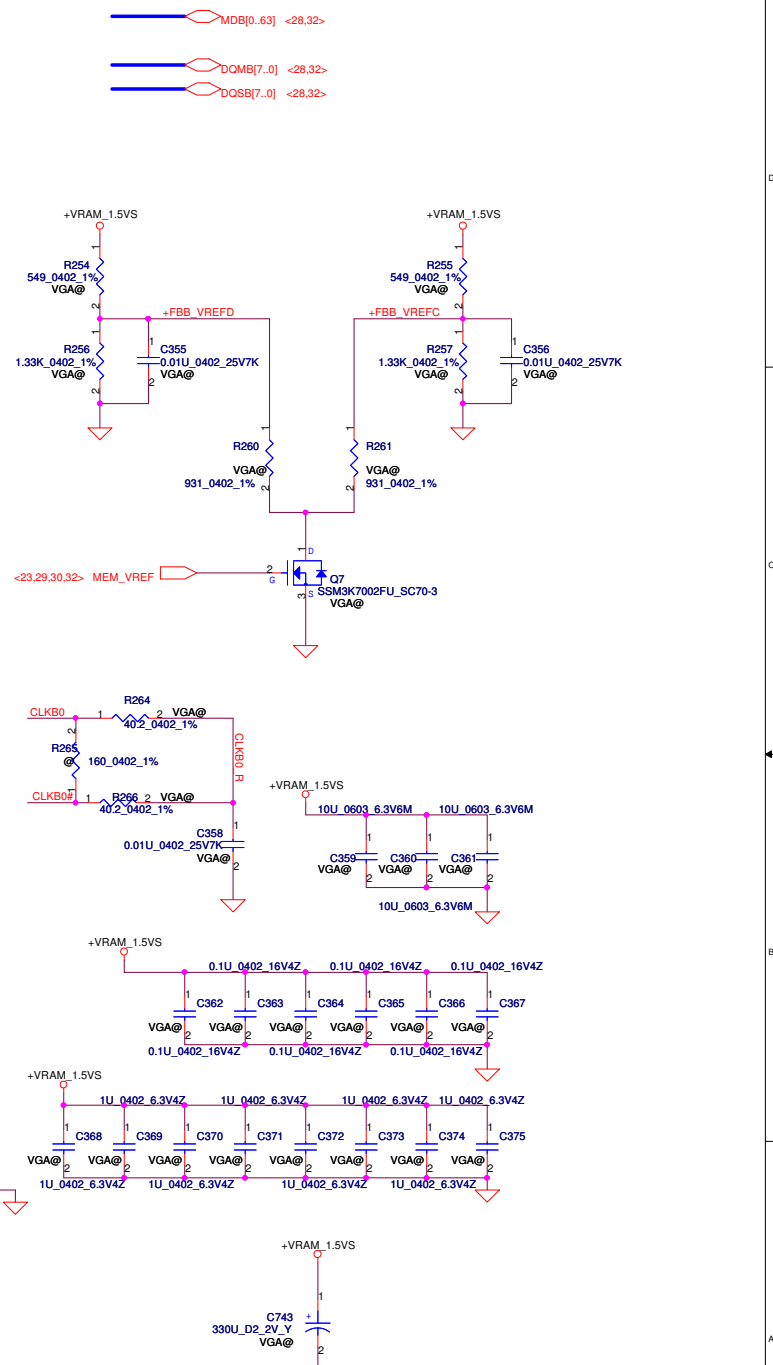
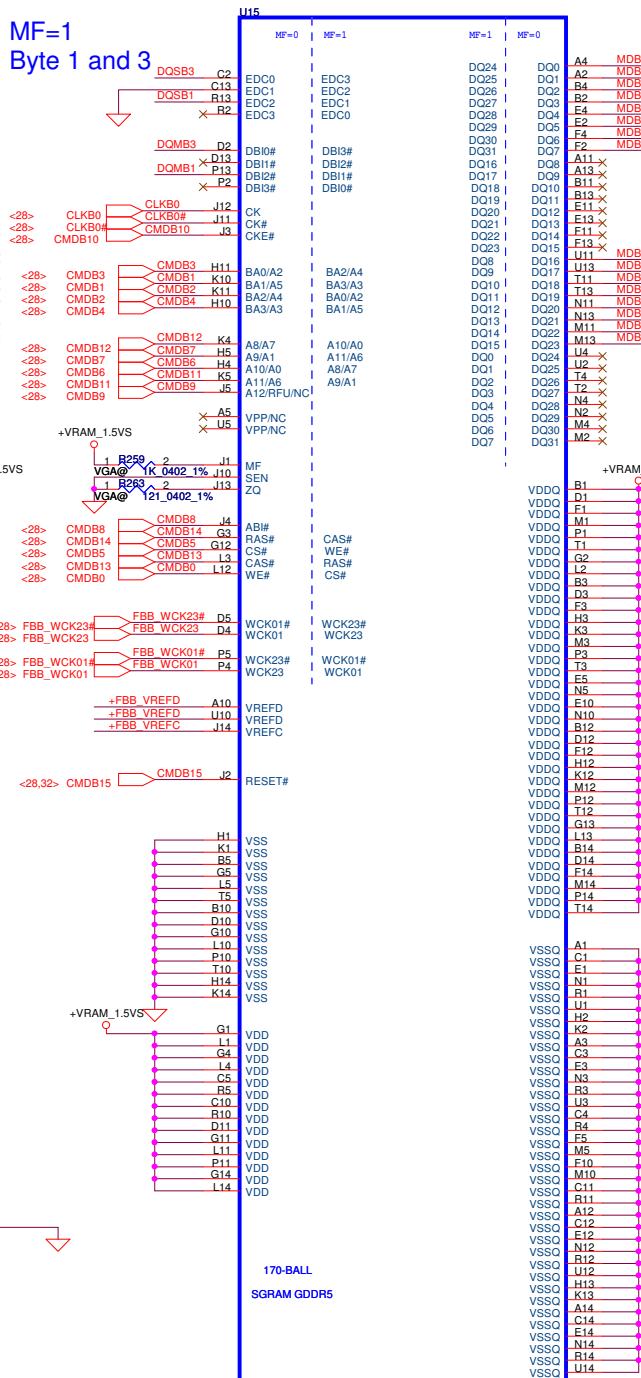


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				Custpm	PLA00 M/B LA-6951P Schematic ¹
				Date:	Friday, September 10, 2010
				Sheet	30 of 66

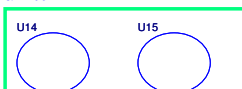
MF=0
Byte 0 and 2



MF=1
Byte 1 and 3



9/7 Add



H5GQ1H24AFR-T2L_BGA170

X76_HYN@

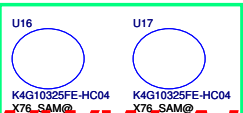
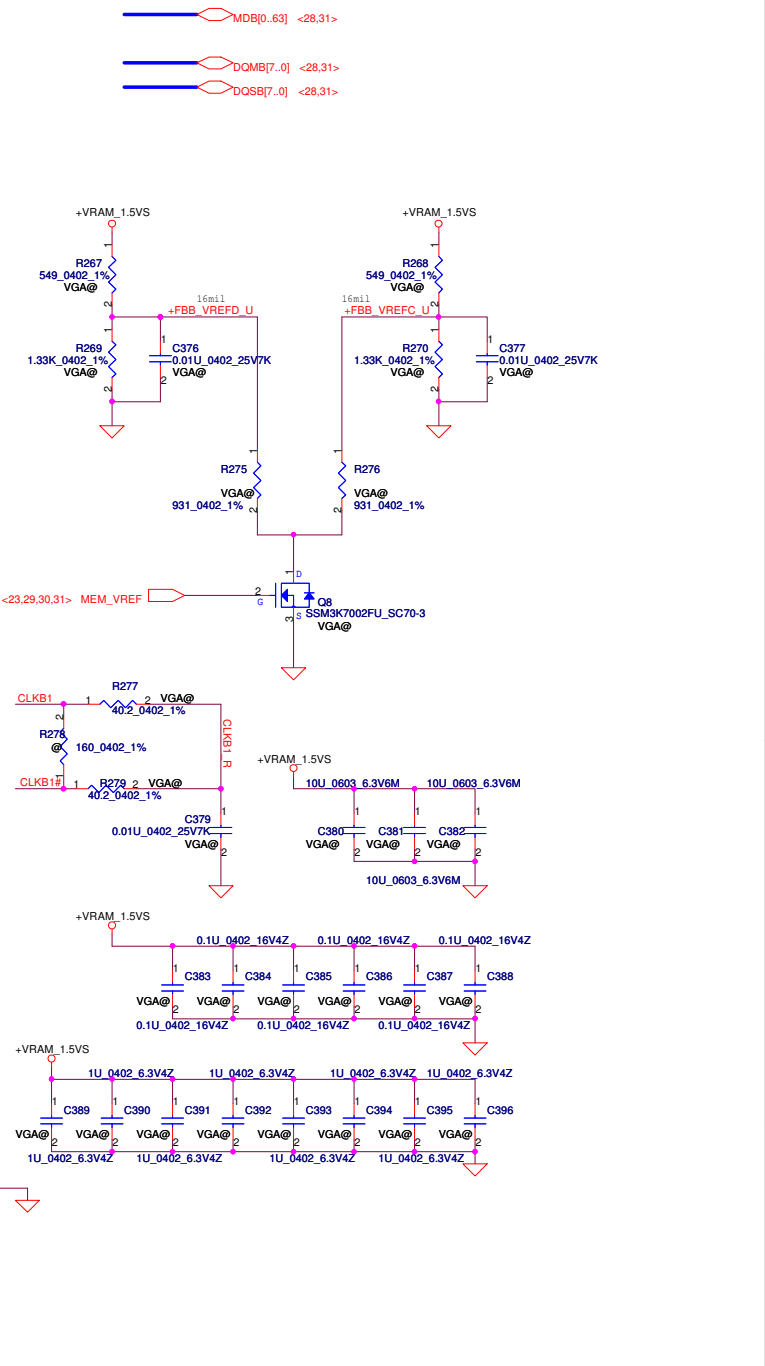
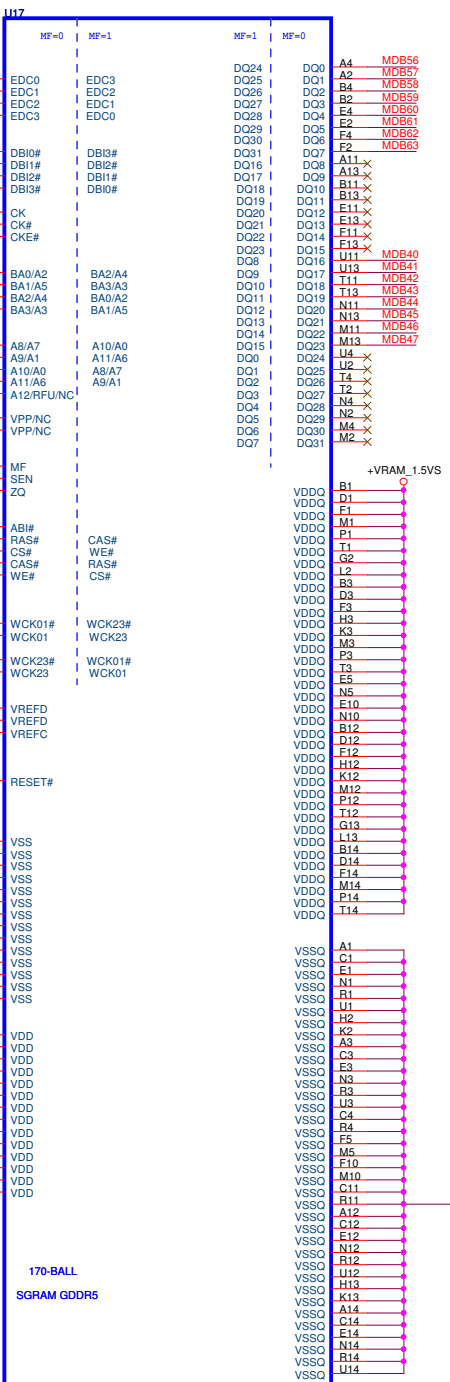
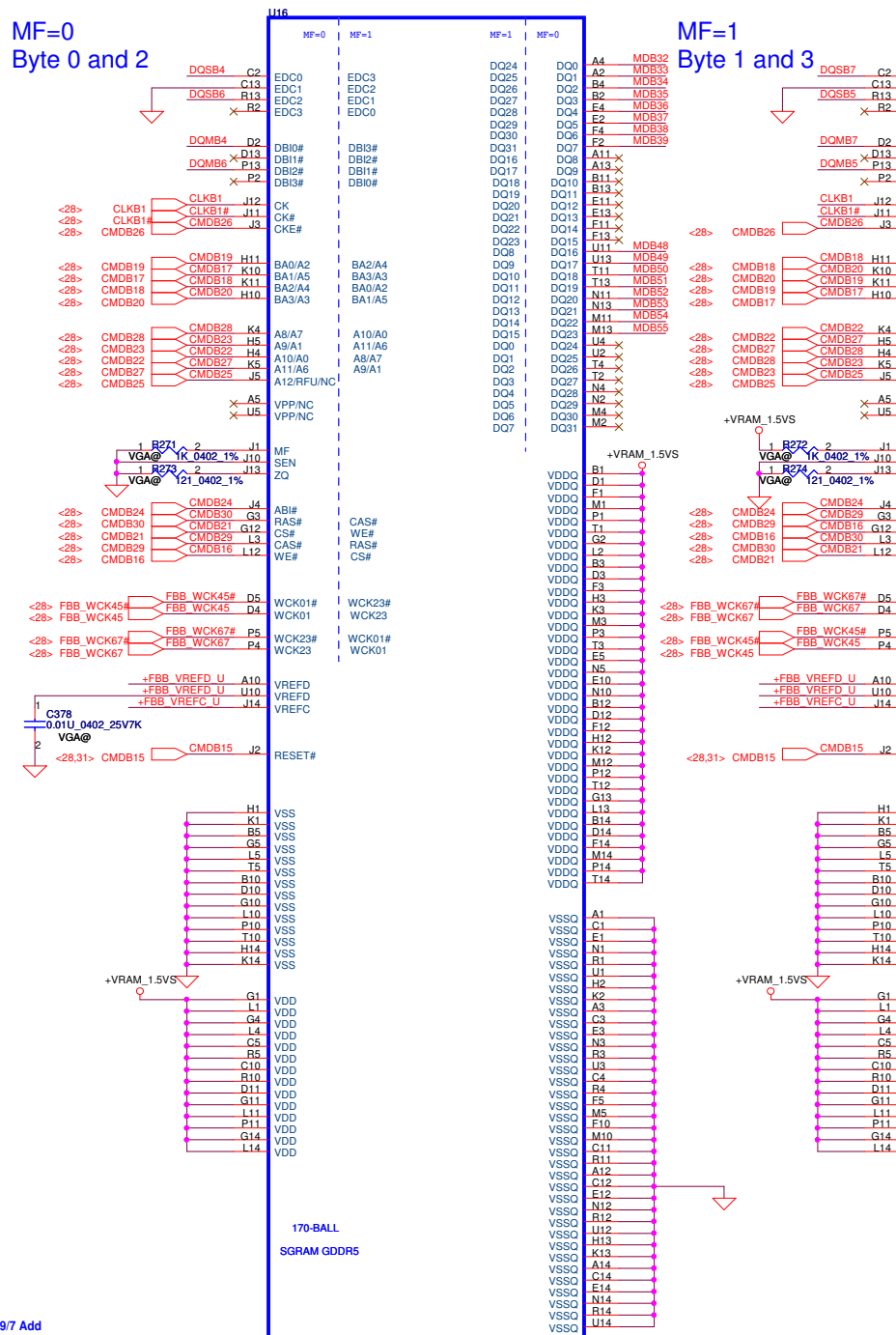
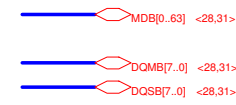
H5GQ1H24AFR-T2L_BGA170

X76_HYN@

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				Custom	PLA00 M/B LA-6951P Schematic 0.1
				Date	Friday, September 10, 2010
				Sheet	31 of 66

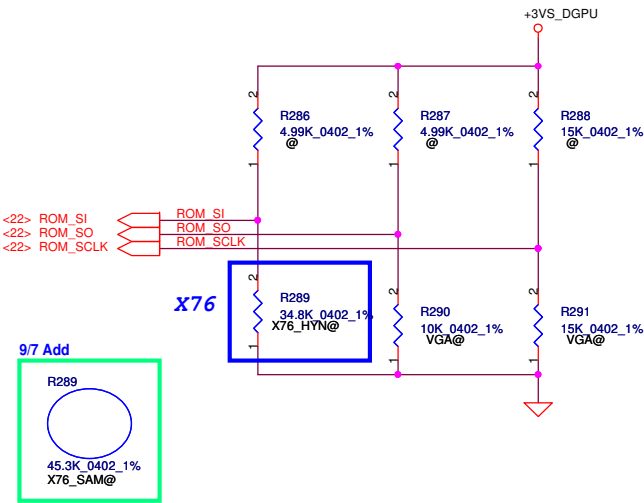
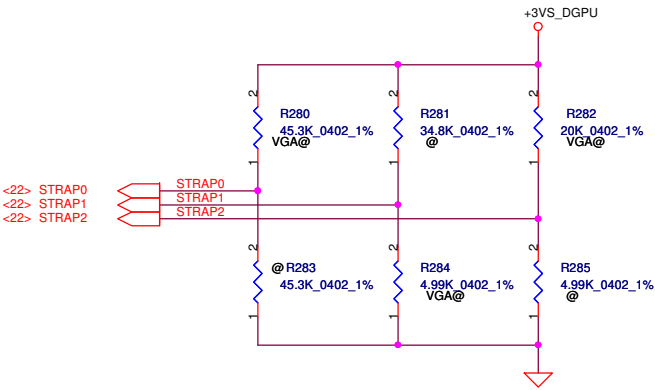
MF=0
Byte 0 and 2

MF=1
Byte 1 and 3



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Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0110	PD 34.8K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0111	PD 45.3K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

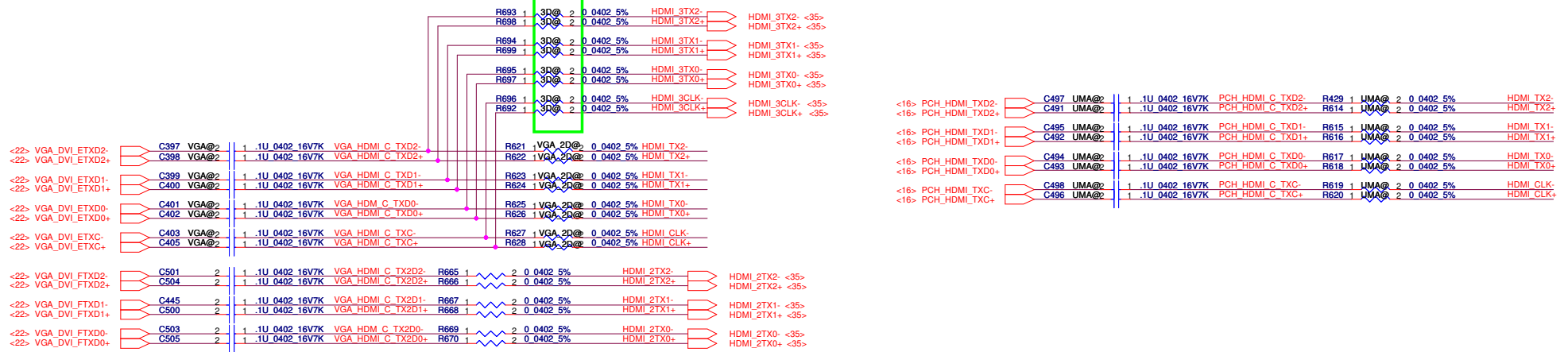
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

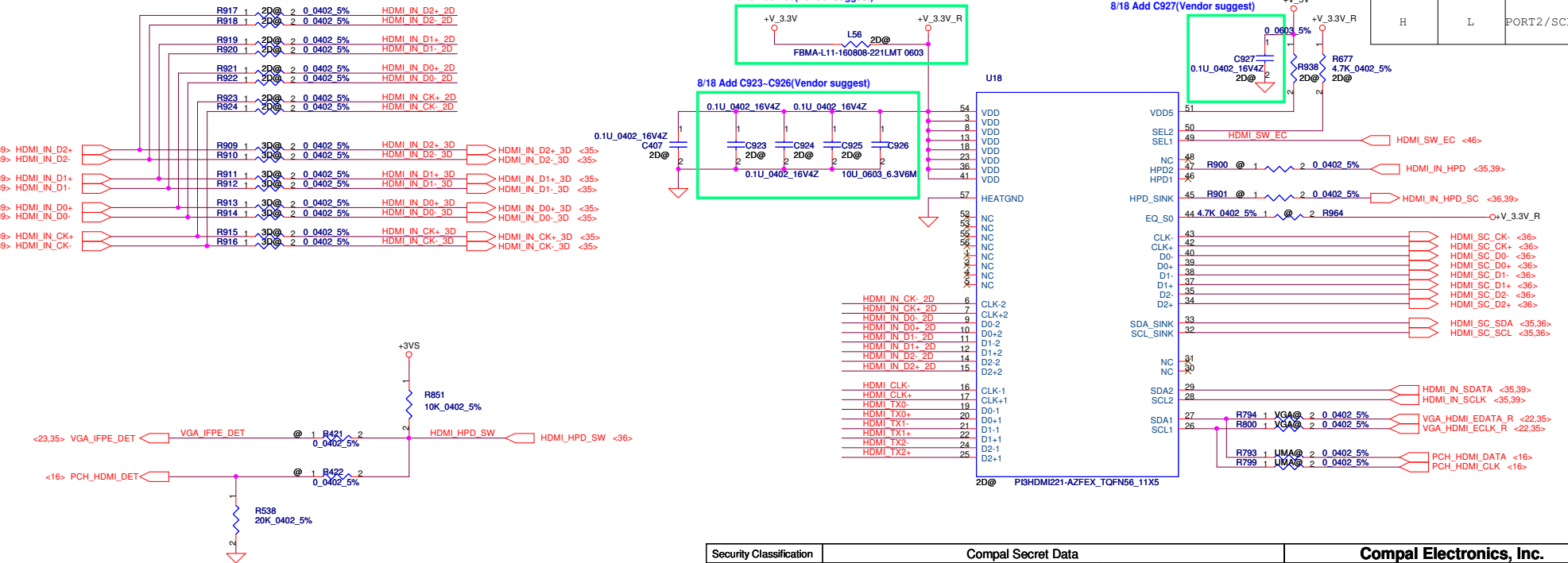
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

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				Custom	PLA00 M/B LA-6951P Schematic	0.1
				Date:	Friday, September 10, 2010	Sheet 33 of 66

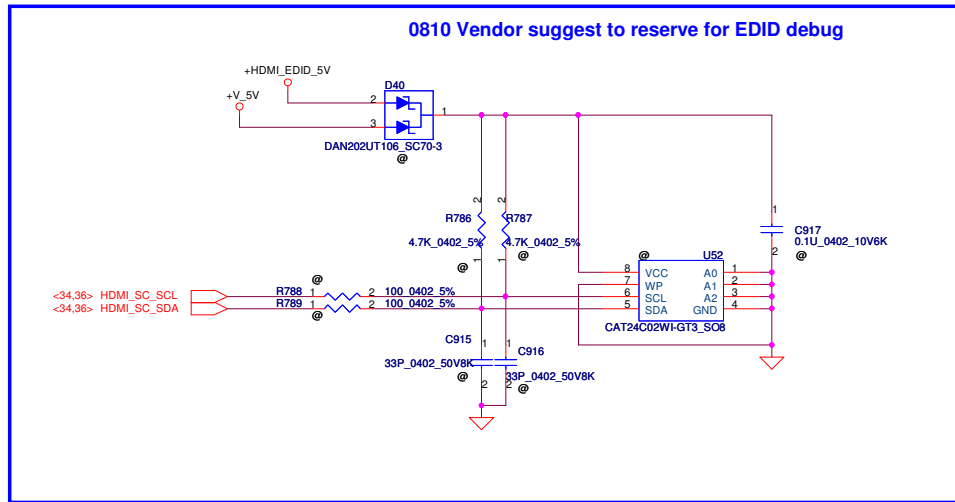
0804 Vendor suggest close to Cap.



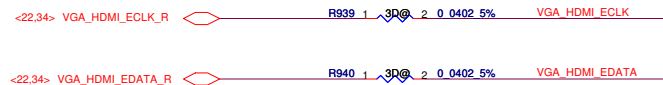
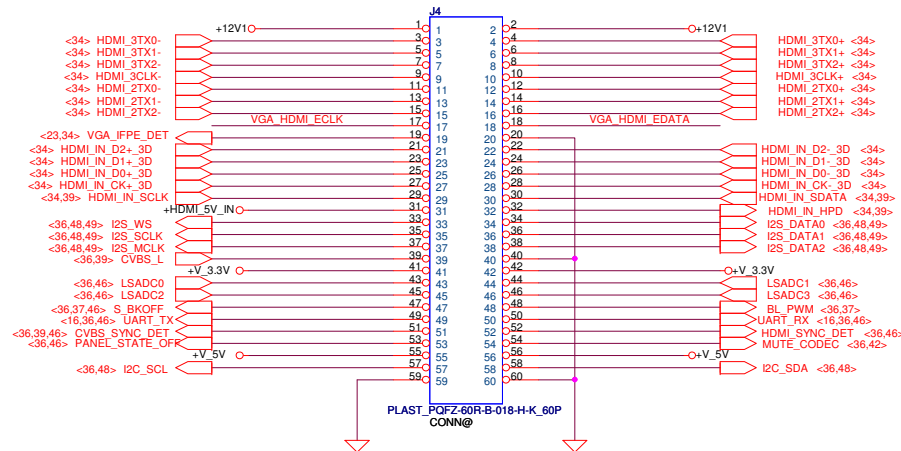
SEL2 (pin50)	SEL1 (pin49)	TMDS/I2C output
H	H	PORT1/SCL1/SDA1
H	L	PORT2/SCL2/SDA2



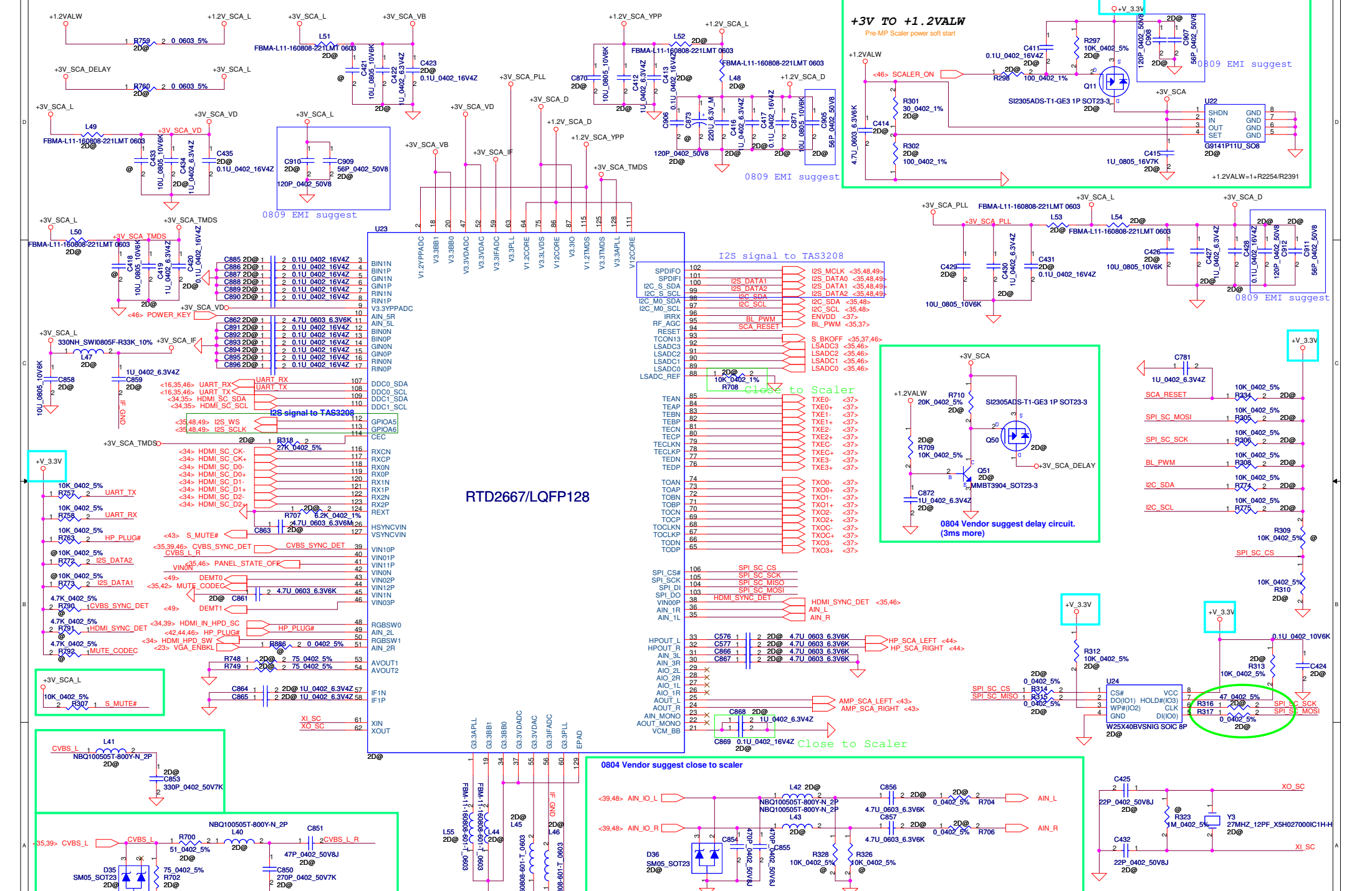
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	HDMI Switch	
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				Date:	Friday, September 10, 2010
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0829 IO/B Pin define update

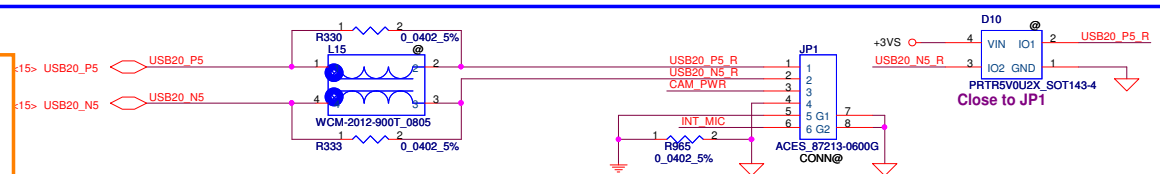


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Issued Date		2010/07/20		Deciphered Date		2011/07/20		
<div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div>				Title				
				3D Scalar				
				Size	Document Number			Rev
				Custom	PLA00 M/B LA-6951P Schematic			0.1
				Date:	Friday, September 10, 2010		Sheet	35



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				Custpm	PLA00 M/B LA-6951P Schematic
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5/18 Change R332 from 100K to 10K ohm

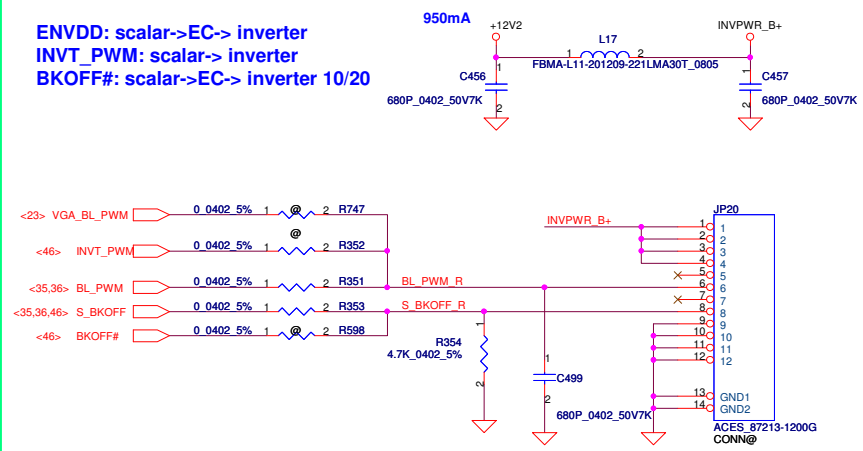


8/15 Add

The schematic diagram shows the microphone input circuit. It starts with a 3V5 supply connected to a 10K resistor (R437). The other end of R437 is connected to the MIC_INT_VREF pin. A 2.2K resistor (R810) is connected between MIC_INT_VREF and the INT_MIC pin. A 0.1uF capacitor (C453) is connected between the INT_MIC pin and ground. A 27K resistor (R809) is connected between the INT_MIC pin and ground. A 1K resistor (R703) is connected between the INT_MIC pin and the INT_MIC_RIGHT pin. A 1K resistor (R705) is connected between the INT_MIC pin and the INT_MIC_LEFT pin. A diode bridge (D41) is connected between the INT_MIC pin and ground. A diode (D42) is connected between the INT_MIC pin and ground.

[illegible][illegible]

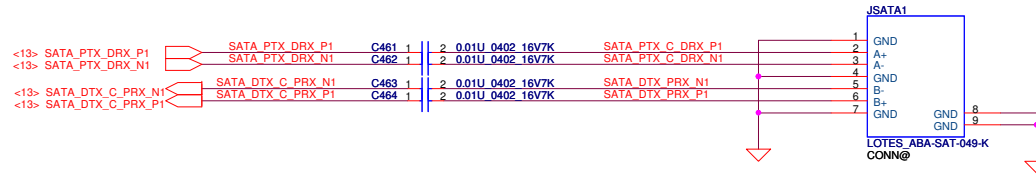
ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20



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					PLA00 M/B LA-6951P Schematic	1	
				Date:	Friday, September 10, 2010	Sheet	37 of 66

HDD

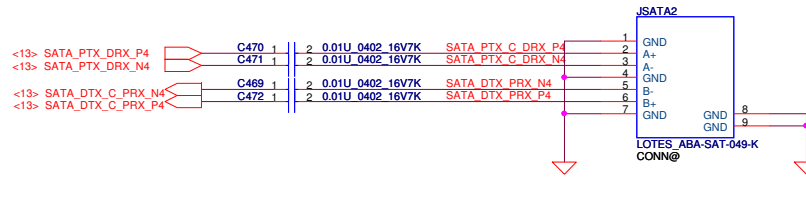
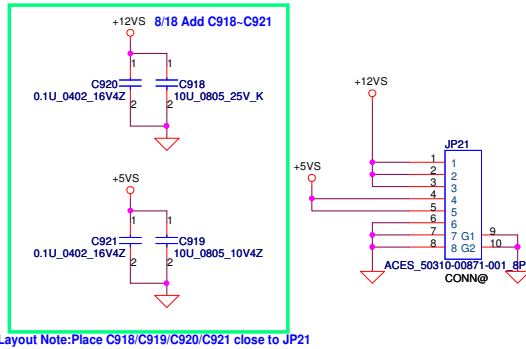
SATA HDD Conn.



HDD/ODD POWER Conn

ODD

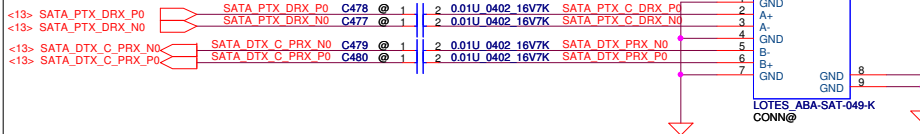
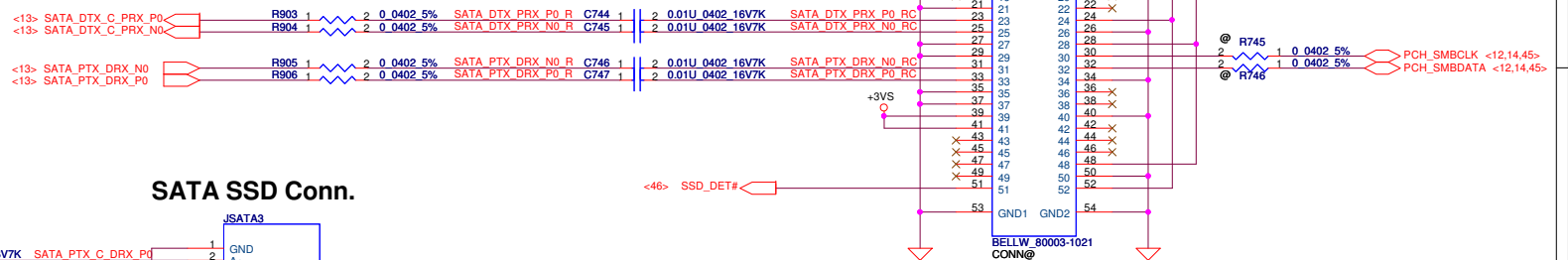
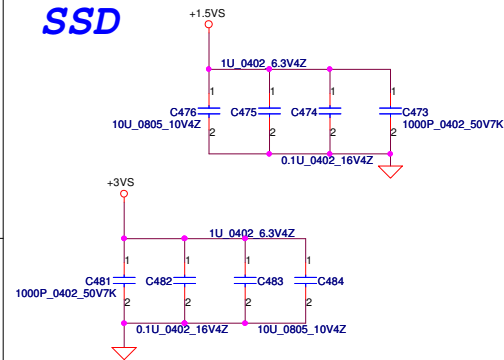
SATA ODD Conn.



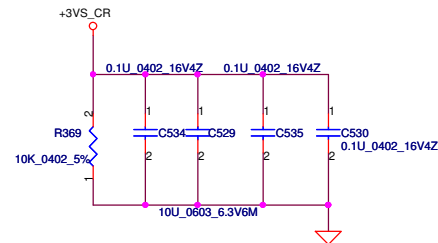
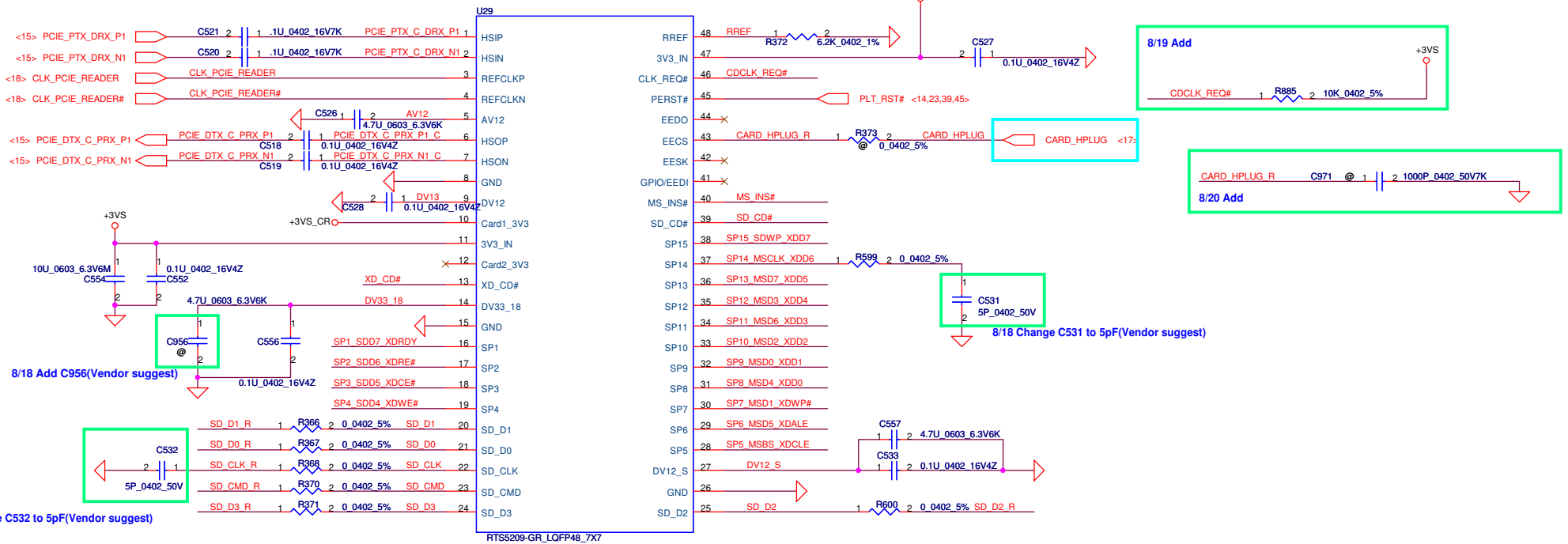
Layout Note: Place C918/C919/C920/C921 close to JP21

SSD

SATA SSD Conn.



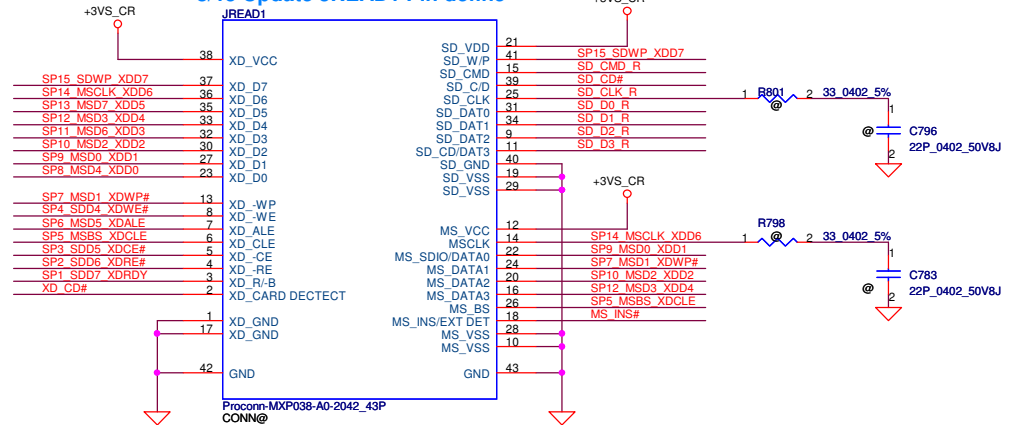
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	B	Document Number	PLA00 M/B LA-6951P Schematic	Rev	0.1
Date:	Friday, September 10, 2010	Sheet	38	of	66



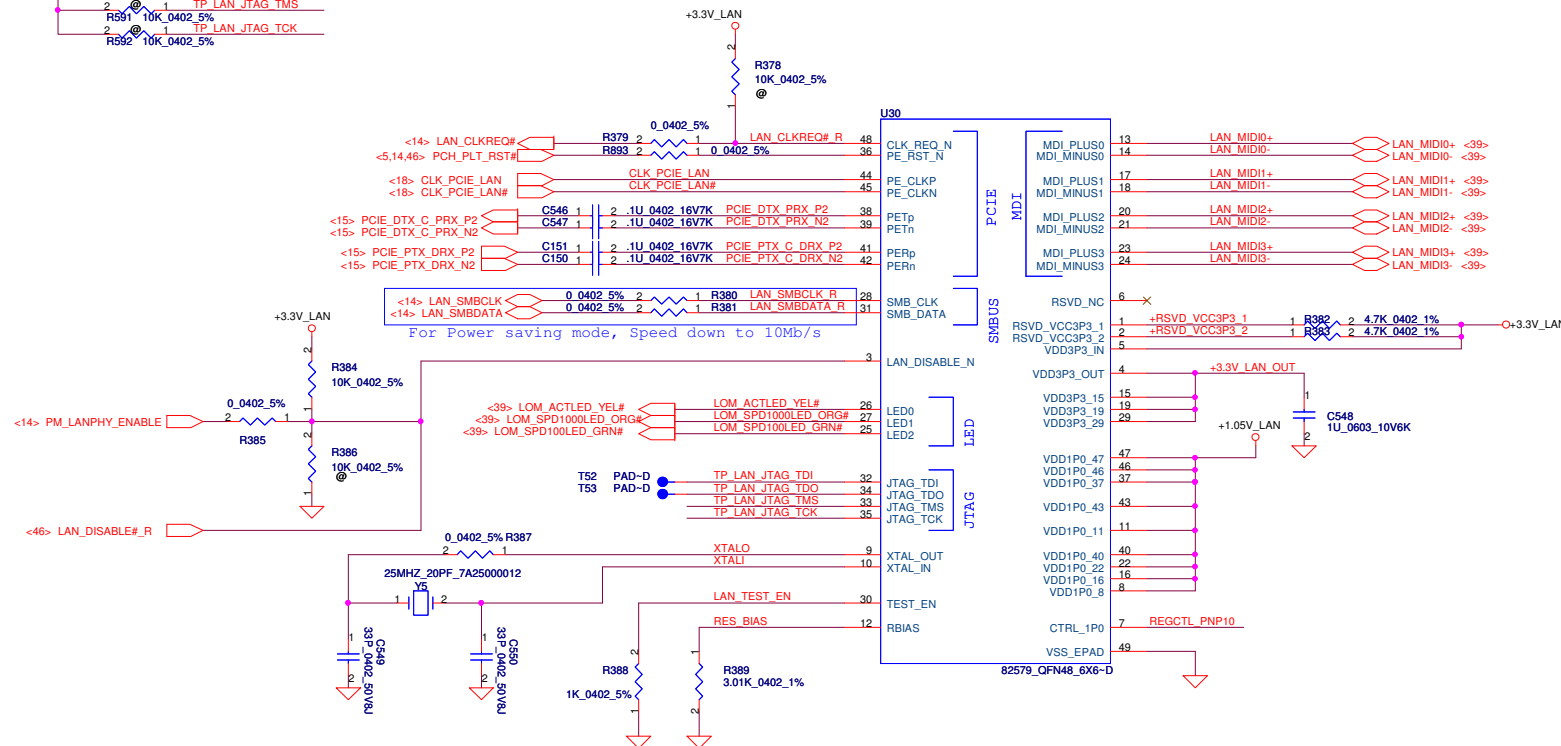
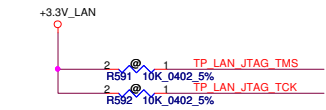
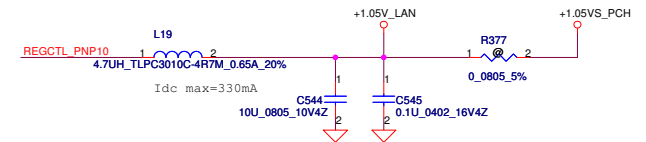
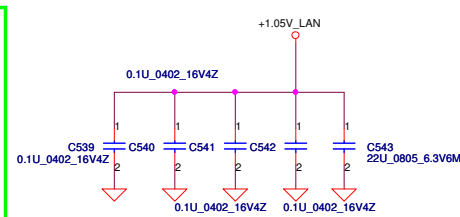
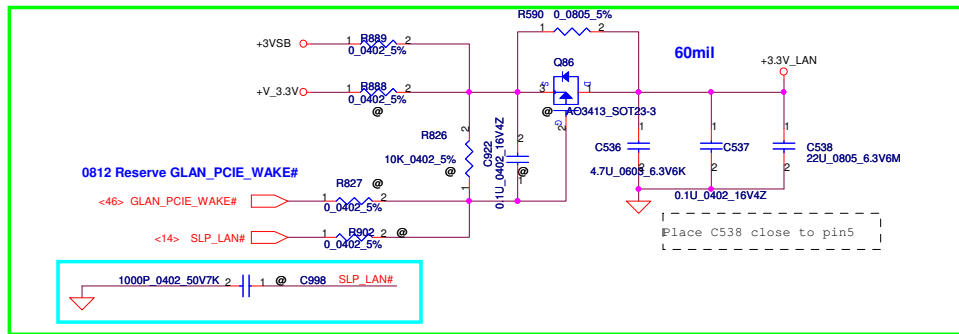
Place C534 close to socket pin 38
Place C529 close to socket pin 21
Place C535 close to socket pin 21
Place C530 close to socket pin 12

< 7 in 1 Card Reader >

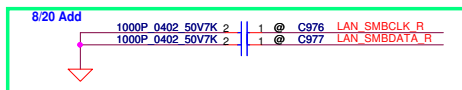
8/15 Update JREAD1 Pin define



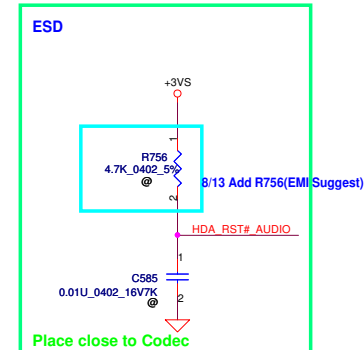
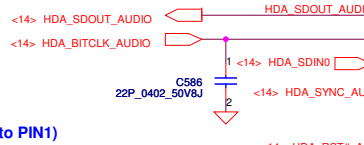
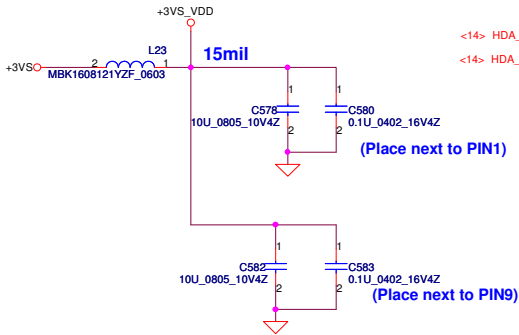
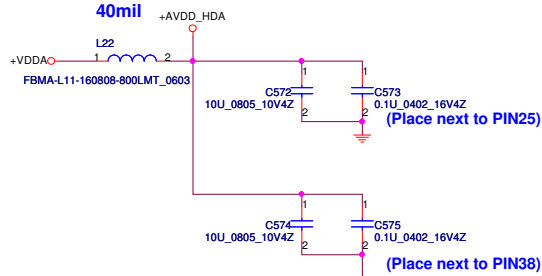
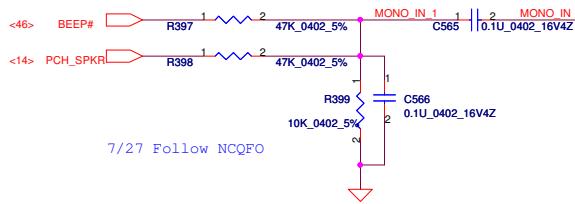
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title PCIE-Card Reader-RTS5209				
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				PLA00 M/B LA-6951P Schematic			c	0.1
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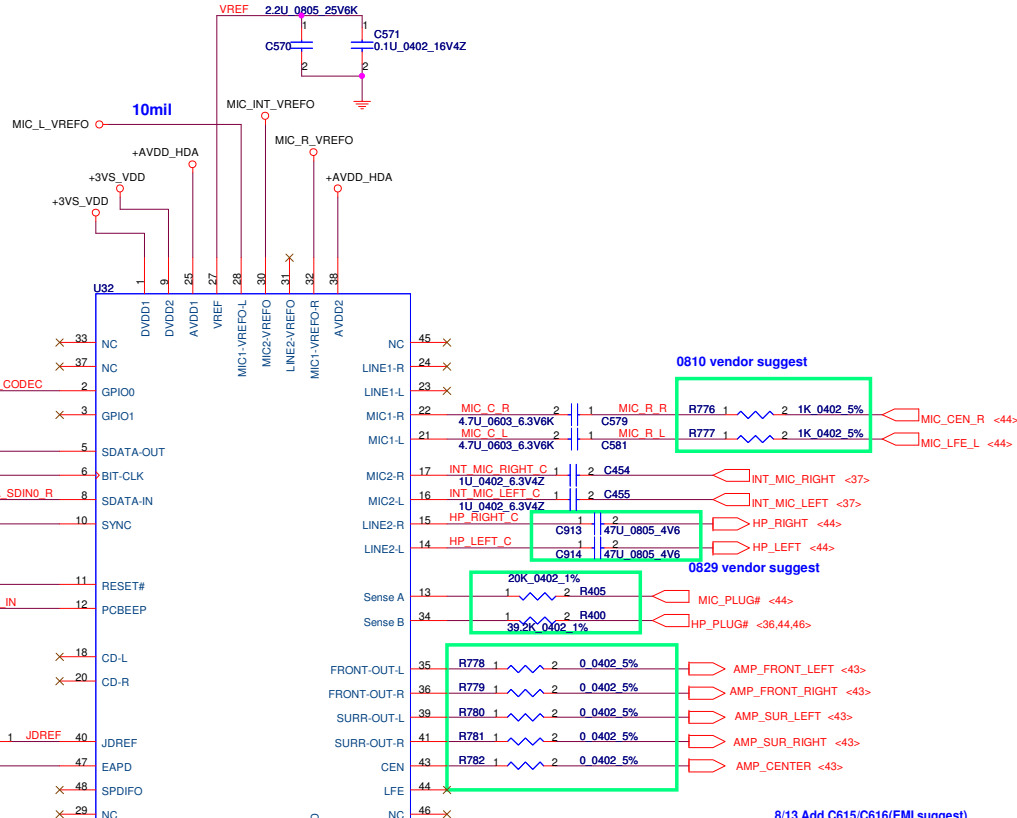
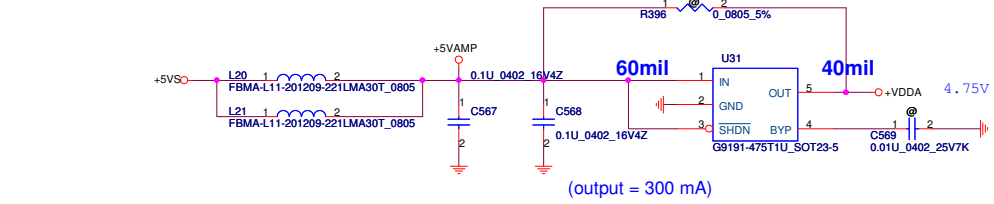
+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	*Internal SRV
STUFF: R377 NO STUFF: L19	STUFF: L19 NO STUFF: R377



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				Date	Friday, September 10, 2010
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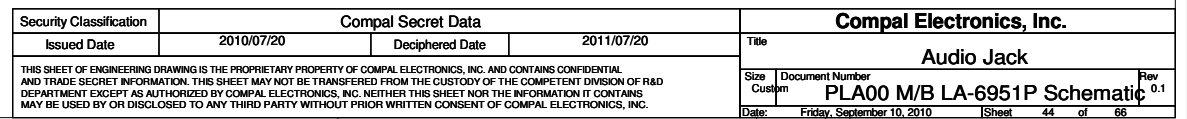
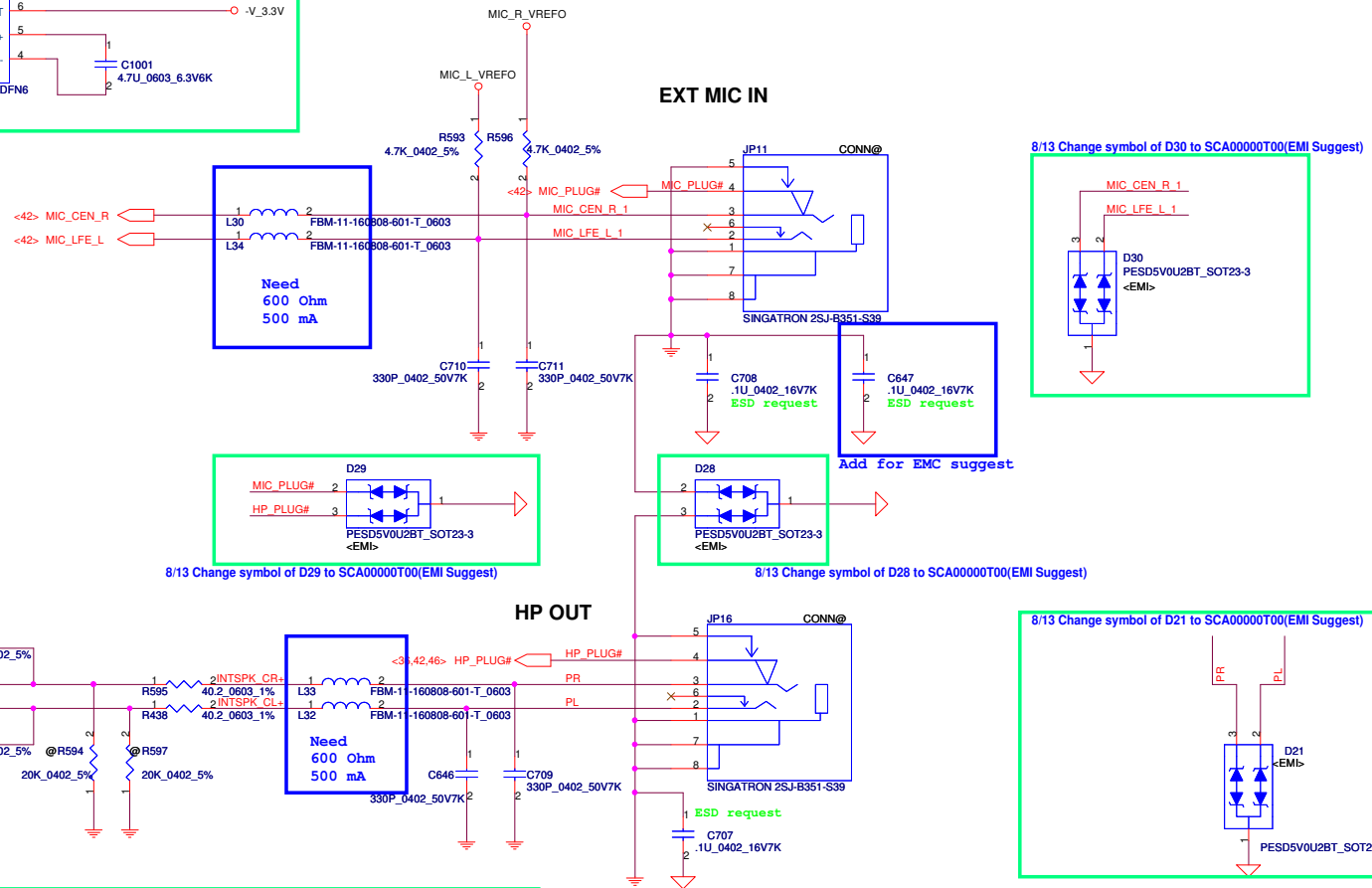
Sense Pin	Impedance	Codec Signals
SENSE A	10K	PORT1 (PIN 23, 24)
SENSE B	20K	PORT-2 (PIN 16, 17)



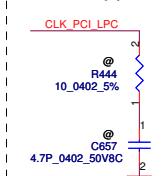
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2010/07/20		Deciphered Date		2011/07/20		Title	
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		Size B	Document Number						Rev
			PLA00 M/B LA-6951P Schematic						0.1
		Date:	Friday, September 10, 2010		Sheet	42	of	66	



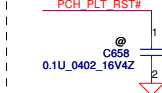
Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1
Date:	Friday, September 10, 2010	Sheet 43 of 66



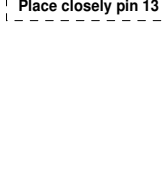
Place closely pin 12



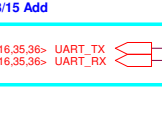
Place closely pin 13



Place closely pin 13



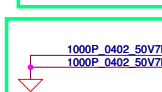
8/15 Add



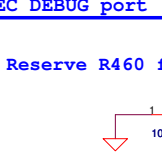
8/19 Add R884(Vendor suggest)



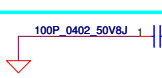
8/20 Add



EC DEBUG port



Reserve R460 for EC debug.



100P 0402 50V8J



ON/OFF



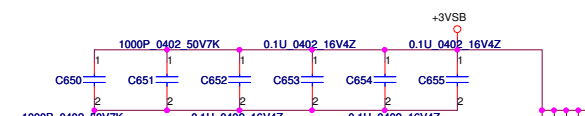
32.768KHZ 12.5PF Q13MC14610002



<14> PCH_SUSCLK



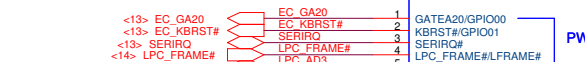
664 15P 0402 50V8J



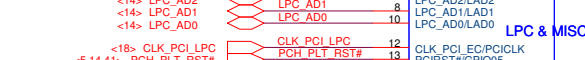
1000P 0402 50V7K



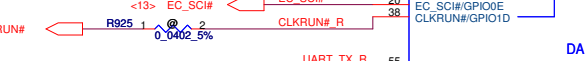
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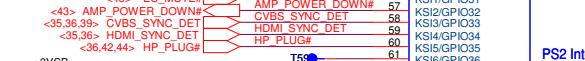
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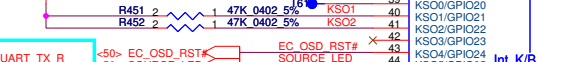
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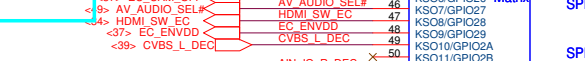
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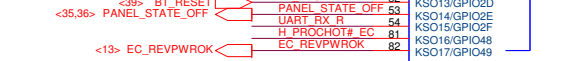
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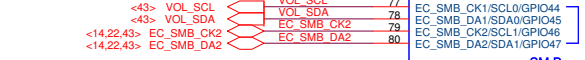
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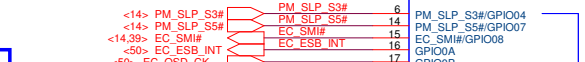
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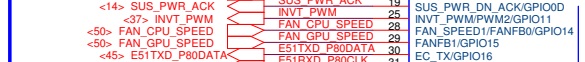
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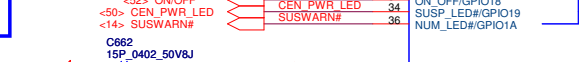
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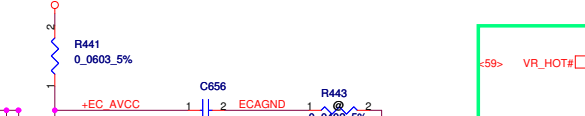
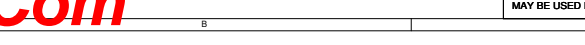
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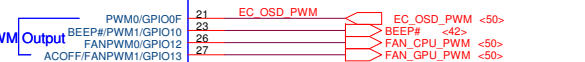
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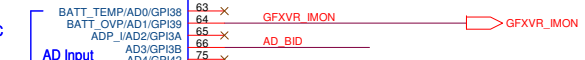
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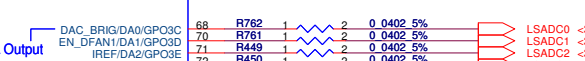
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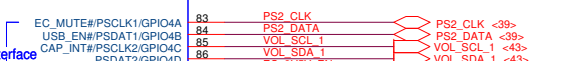
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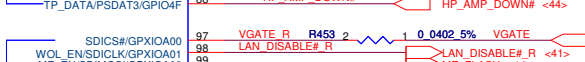
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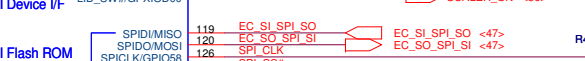
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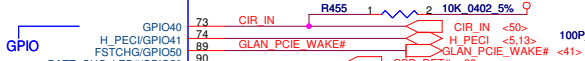
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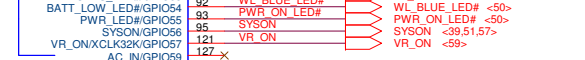
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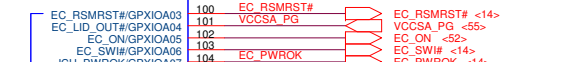
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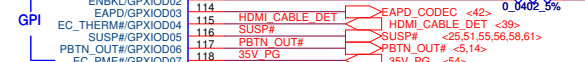
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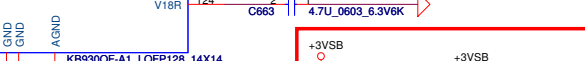
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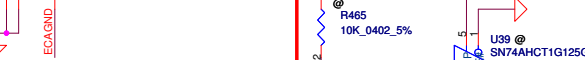
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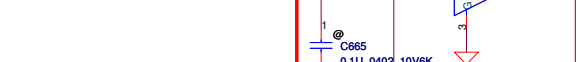
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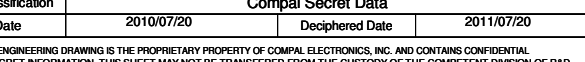
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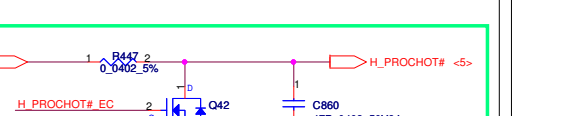
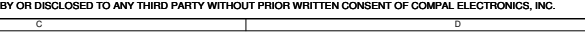
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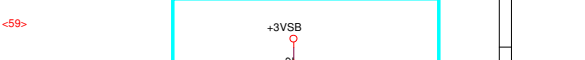
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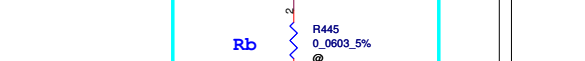
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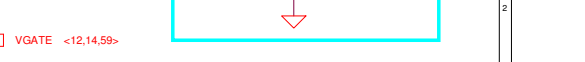
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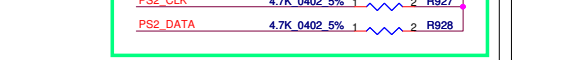
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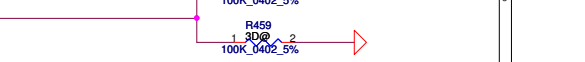
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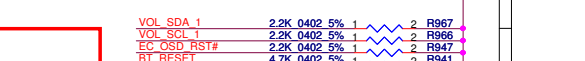
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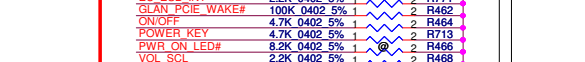
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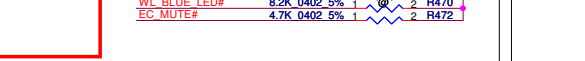
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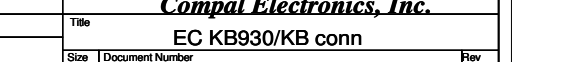
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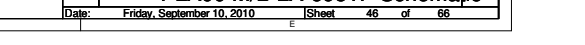
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0.1U 0402 16V4Z

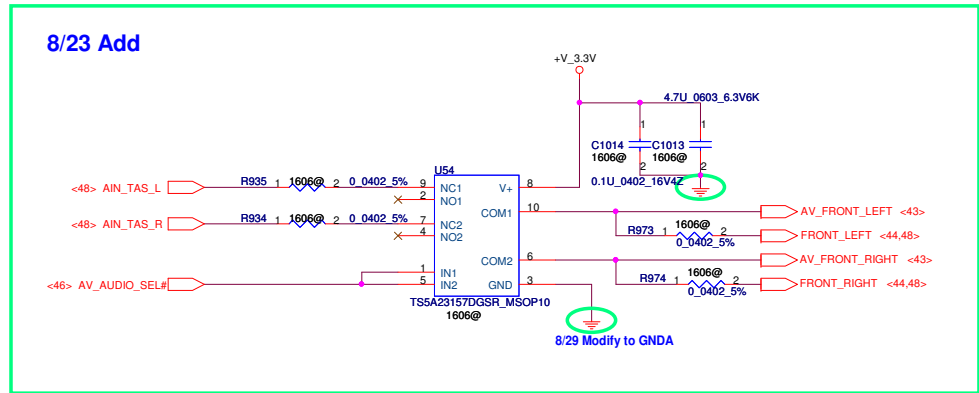
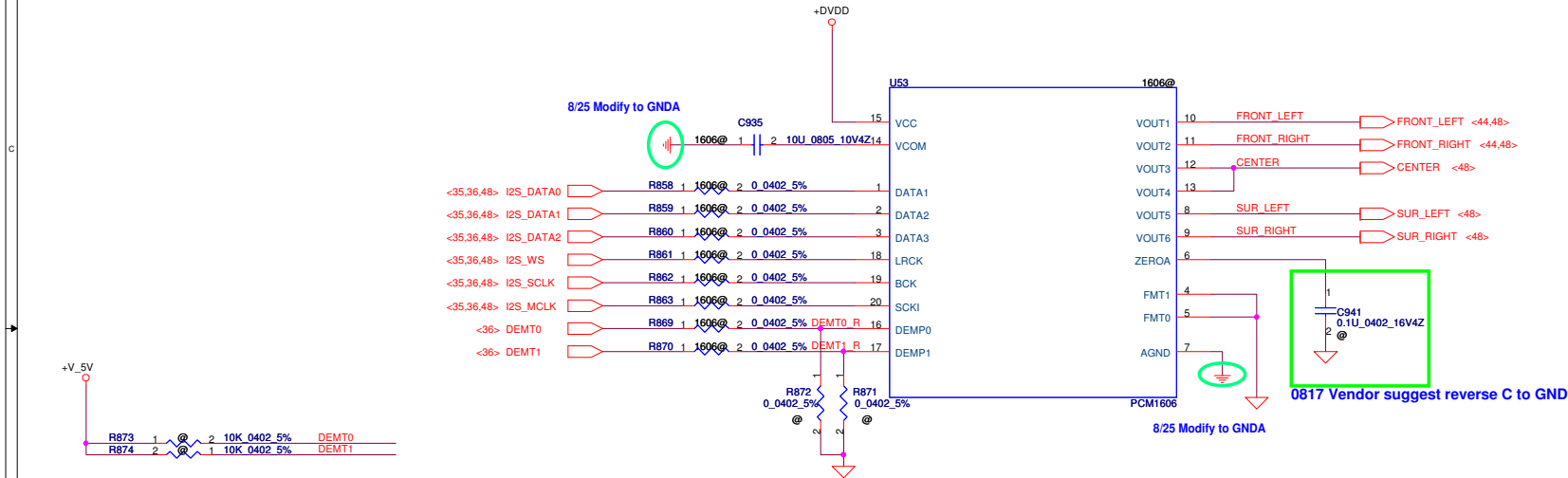


0.1U 0402 16V4Z



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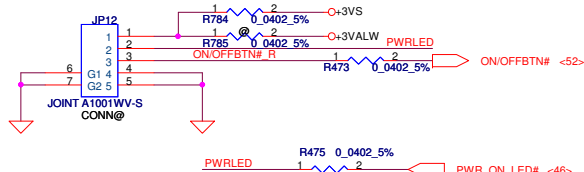




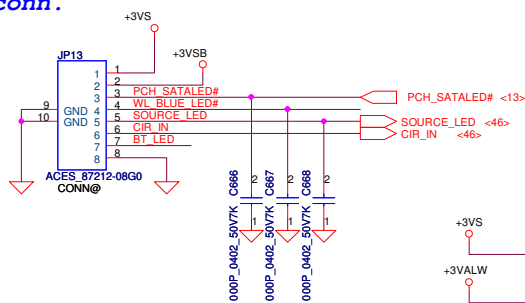
De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

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				Custom	PLA00 M/B LA-6951P Schematic
				Date:	Friday, September 10, 2010
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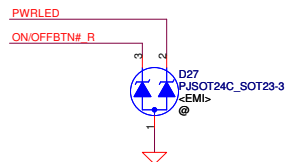
Power switch board



LED board conn.

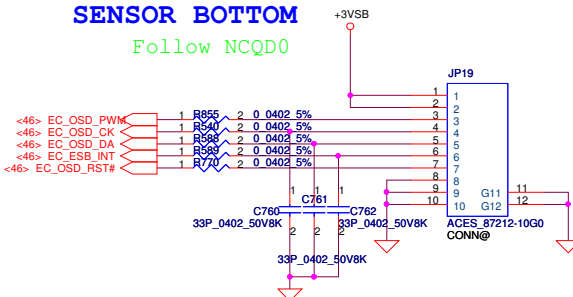


8/13 Change symbol of D27 to SCA0000E00(EMI Suggest)

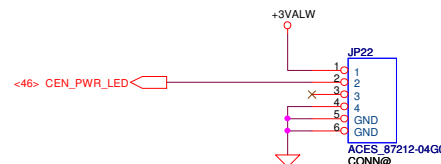


SENSOR BOTTOM

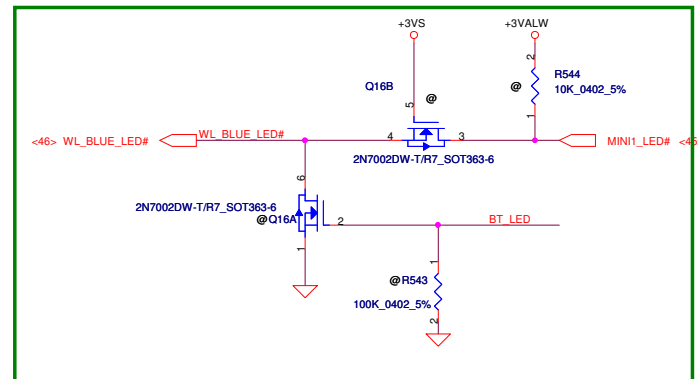
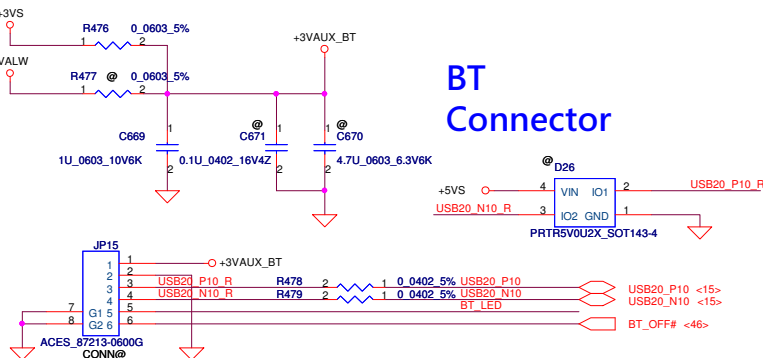
Follow NCQD0



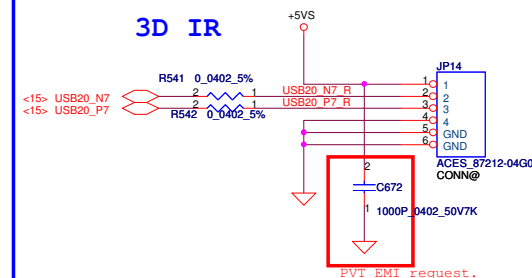
DECO LED board conn.



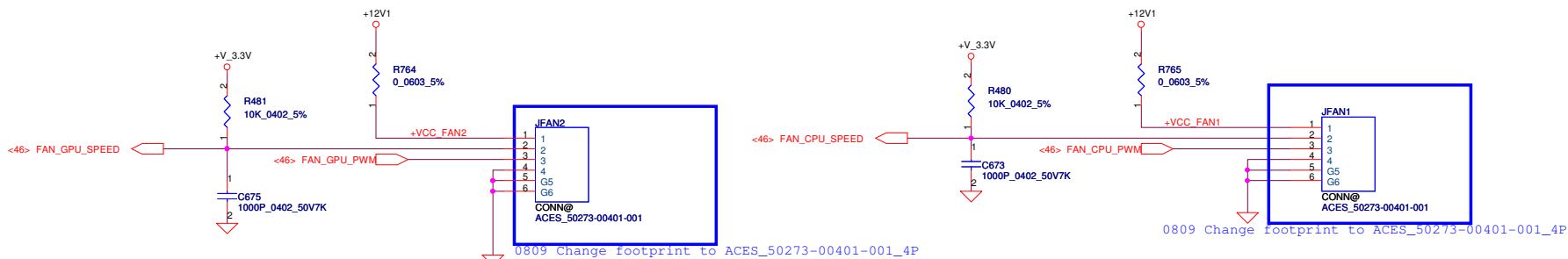
BT Connector



3D IR

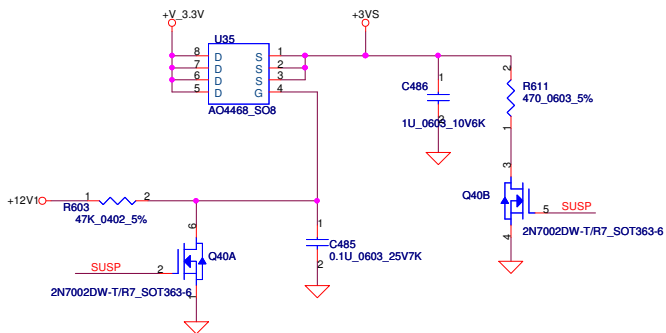


Fan Control circuit

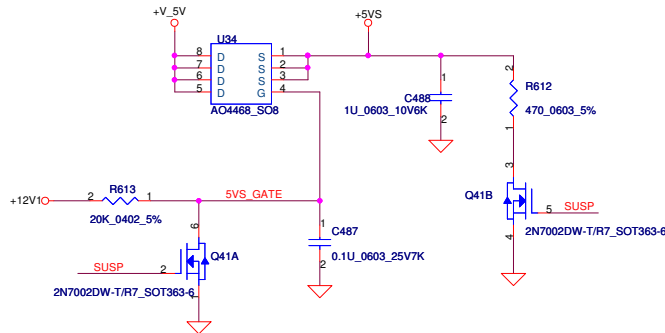


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Size	Document Number	PLA00 M/B LA-6951P Schematic		Rev	0.1
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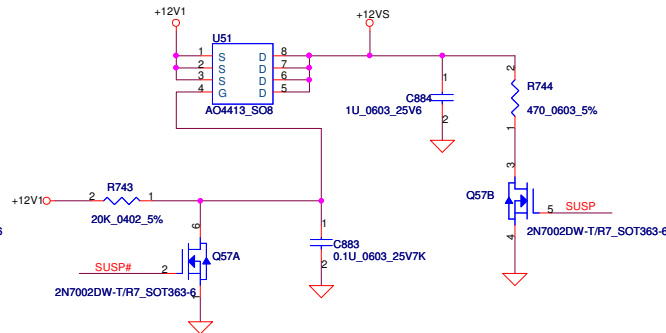
+V_3.3V TO +3VS



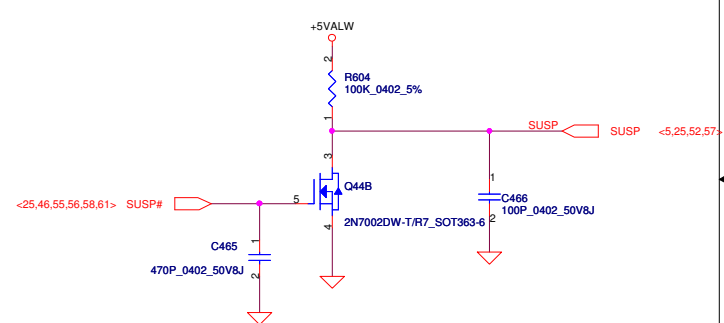
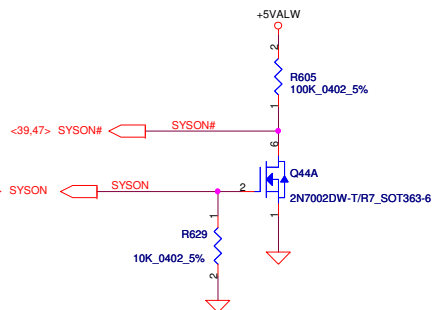
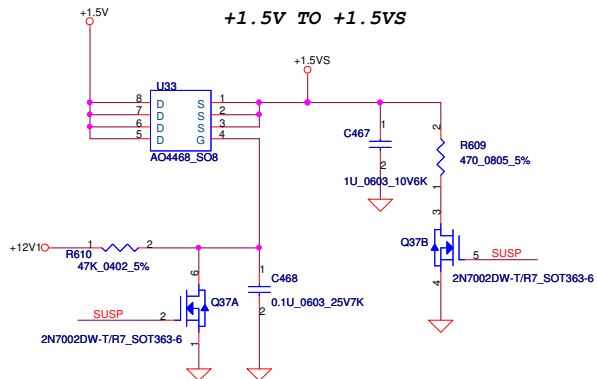
+V_5V TO +5VS



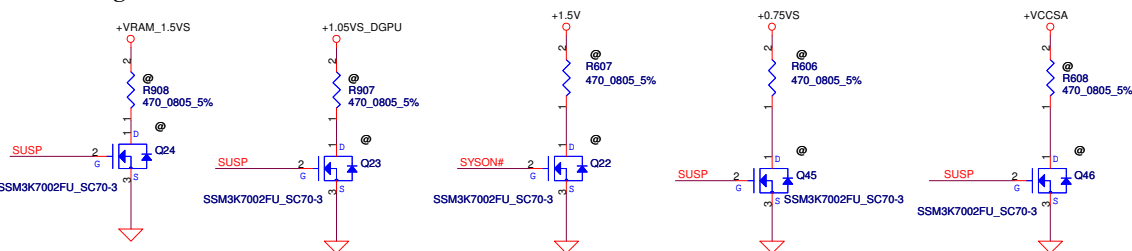
+12V1 TO +12VS



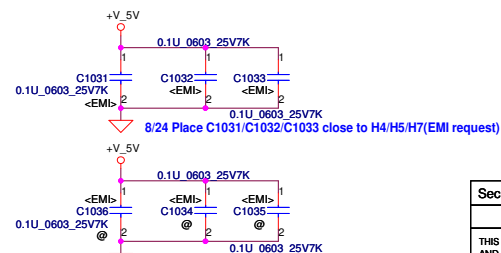
+1.5V TO +1.5VS



Discharge circuit



8/24 Add C1031-C1036



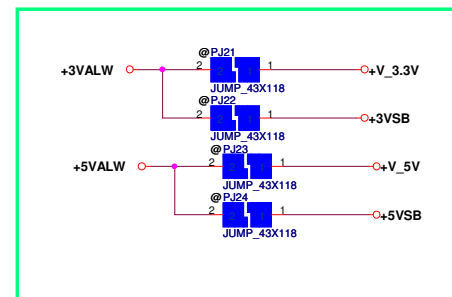
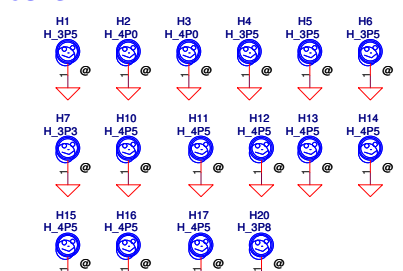
8/24 Place C1031/C1032/C1033 close to H4/H5/H7(EMI request)

8/24 Place C1034/C1035/C1036 close to H1/H2/H6(EMI request)

NON-PDH



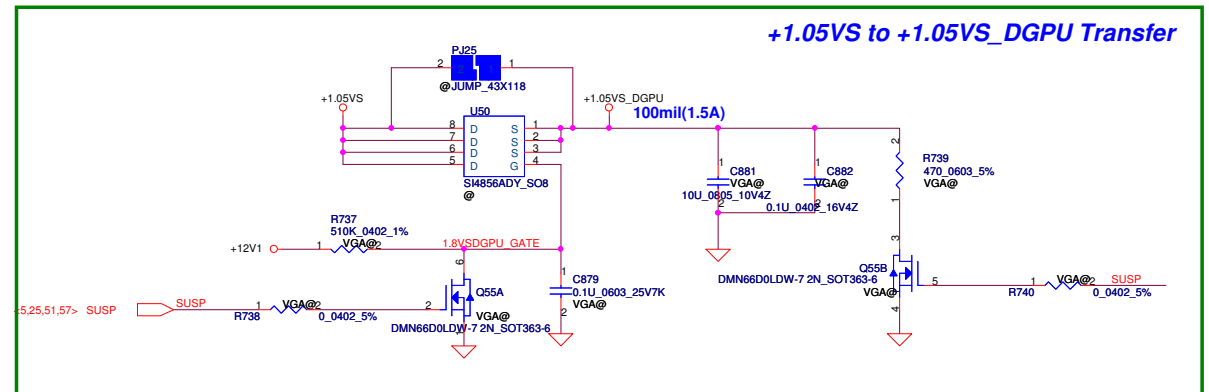
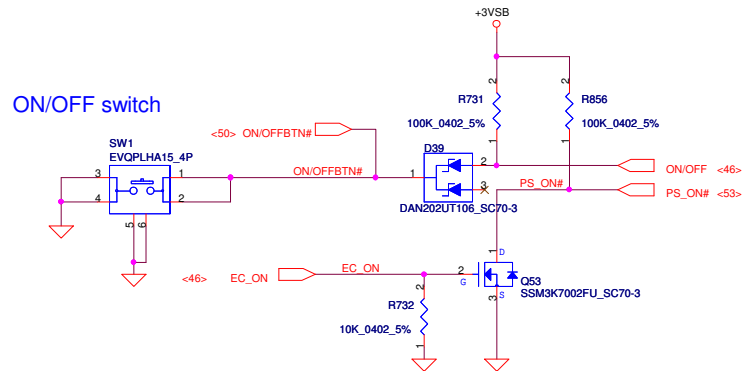
Screw



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Deciphered Date				2011/07/20				DC Interface/Screw			
Size				Document Number				Rev			
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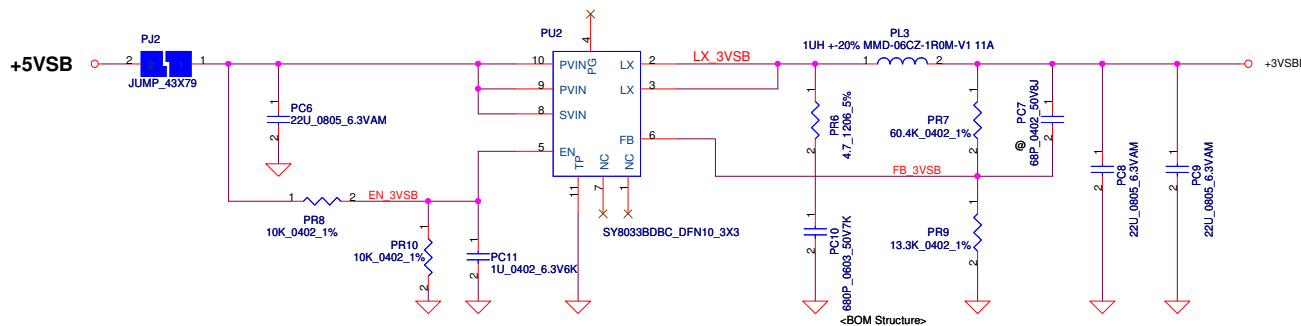
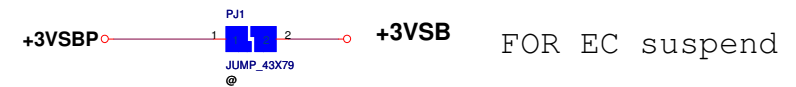
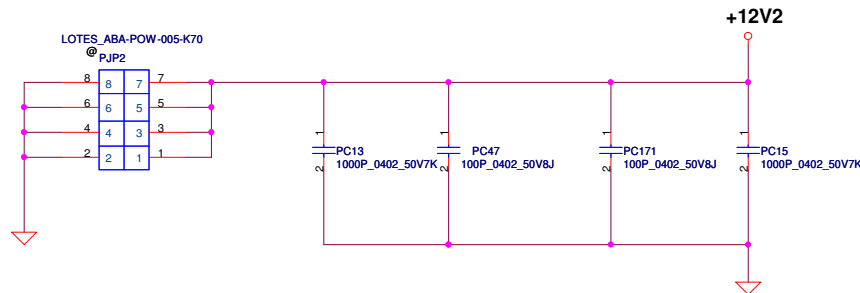
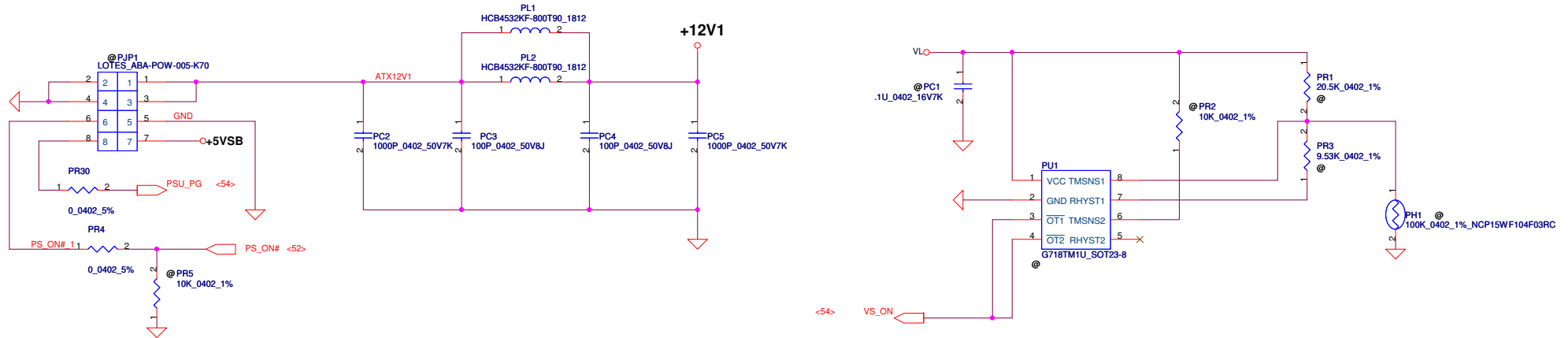
Power Button



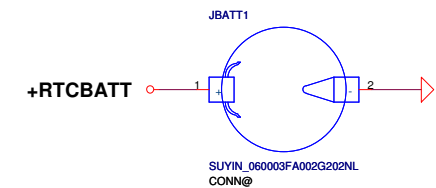
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Size B	Document Number	PLA00 M/B LA-6951P Schematic			Rev 0.1
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PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C



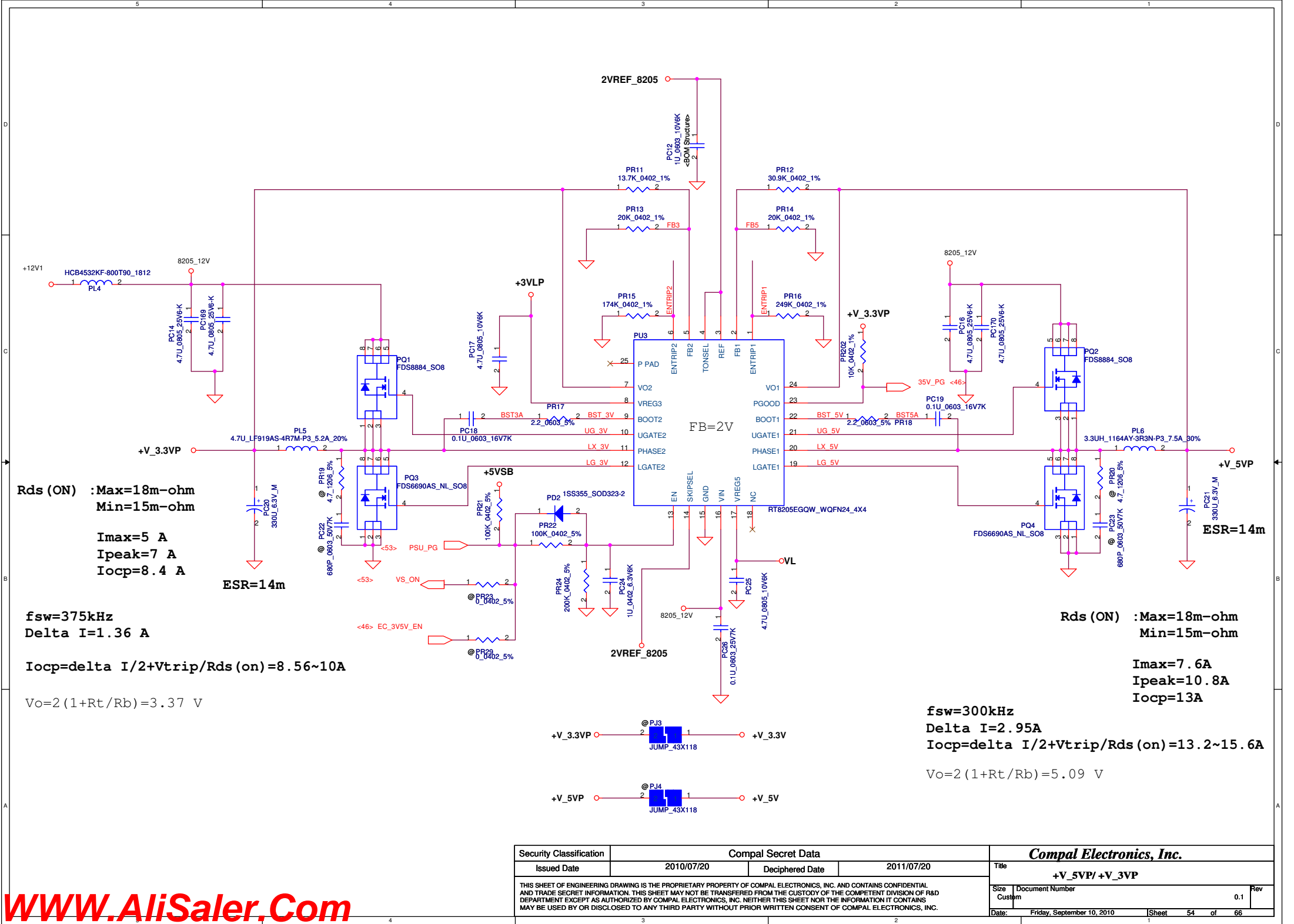
$V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR7/PR9) = 3.318V$
 $I_{peak} = 0.062A, I_{max} = 0.045A$
Current limit >4A



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								Rev			
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Rds (ON) :Max=18m-ohm
Min=15m-ohm

Imax=5 A
Ipeak=7 A
Iocp=8.4 A

fsw=375kHz
Delta I=1.36 A

Iocp=delta I/2+Vtrip/Rds(on)=8.56~10A

Vo=2(1+Rt/Rb)=3.37 V

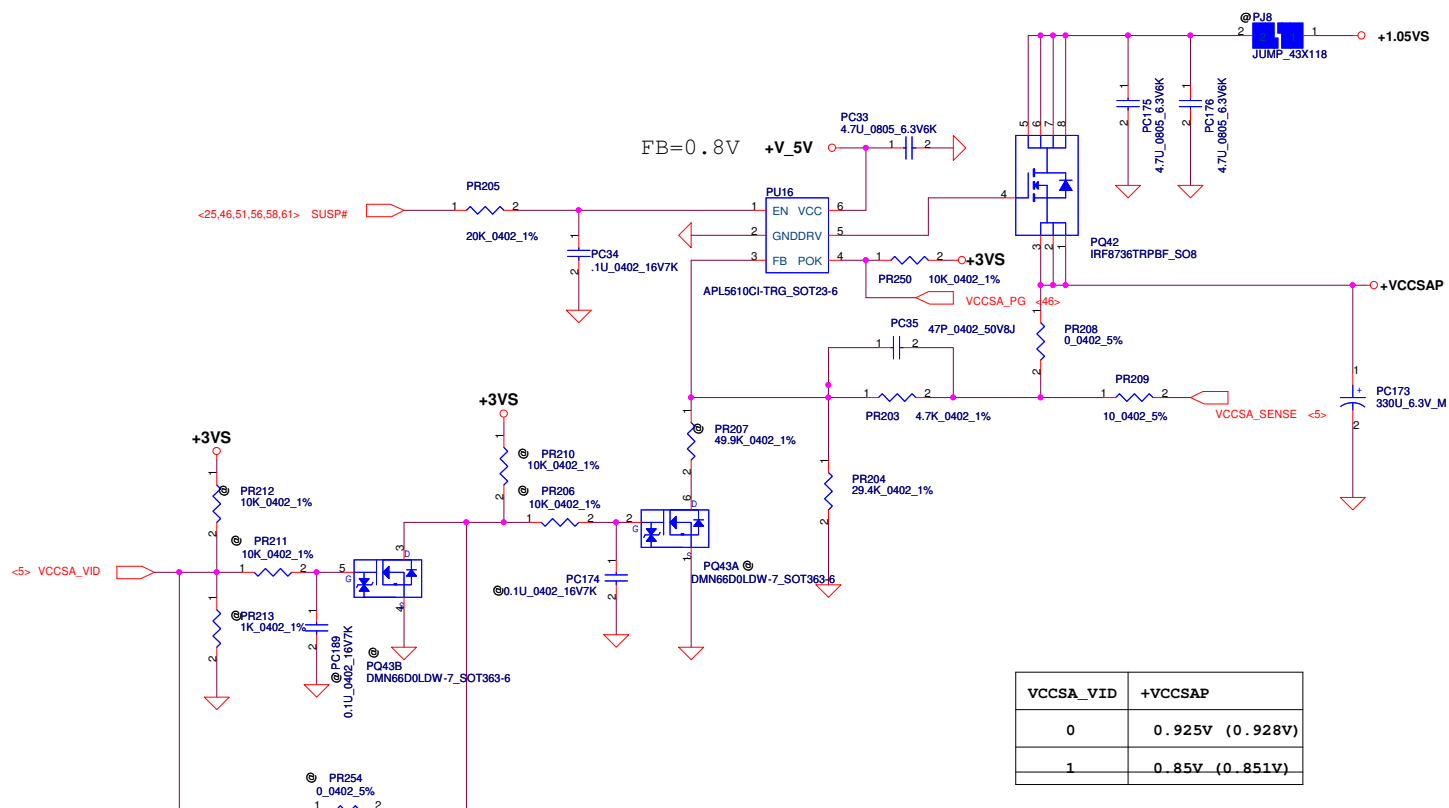
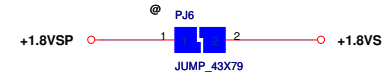
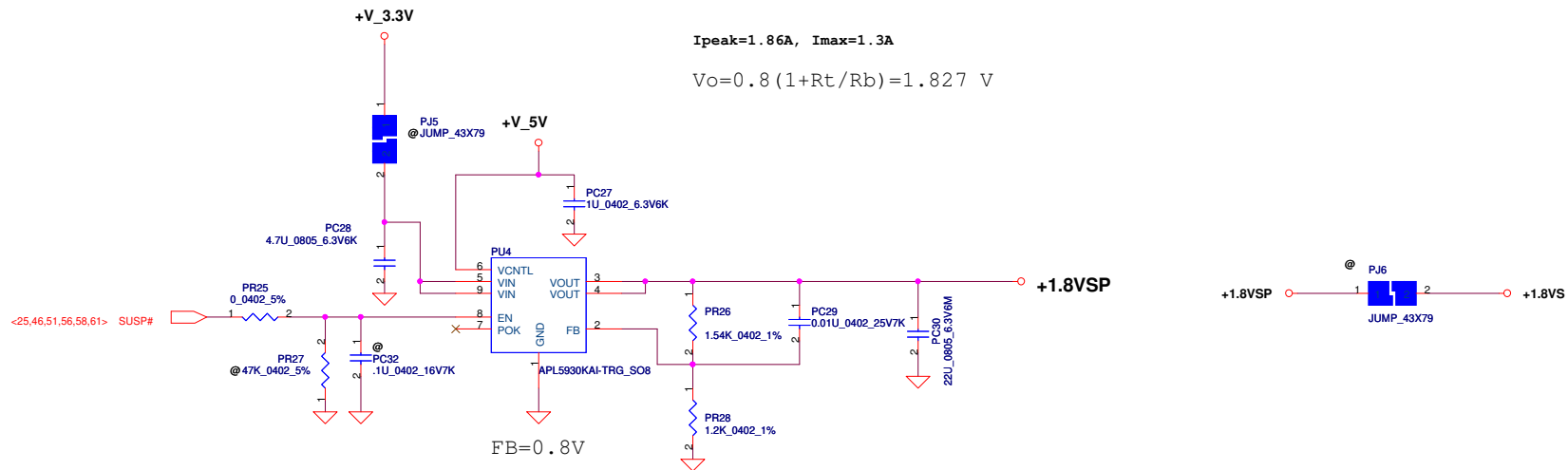
Rds (ON) :Max=18m-ohm
Min=15m-ohm

Imax=7.6A
Ipeak=10.8A
Iocp=13A

fsw=300kHz
Delta I=2.95A
Iocp=delta I/2+Vtrip/Rds(on)=13.2~15.6A

Vo=2(1+Rt/Rb)=5.09 V

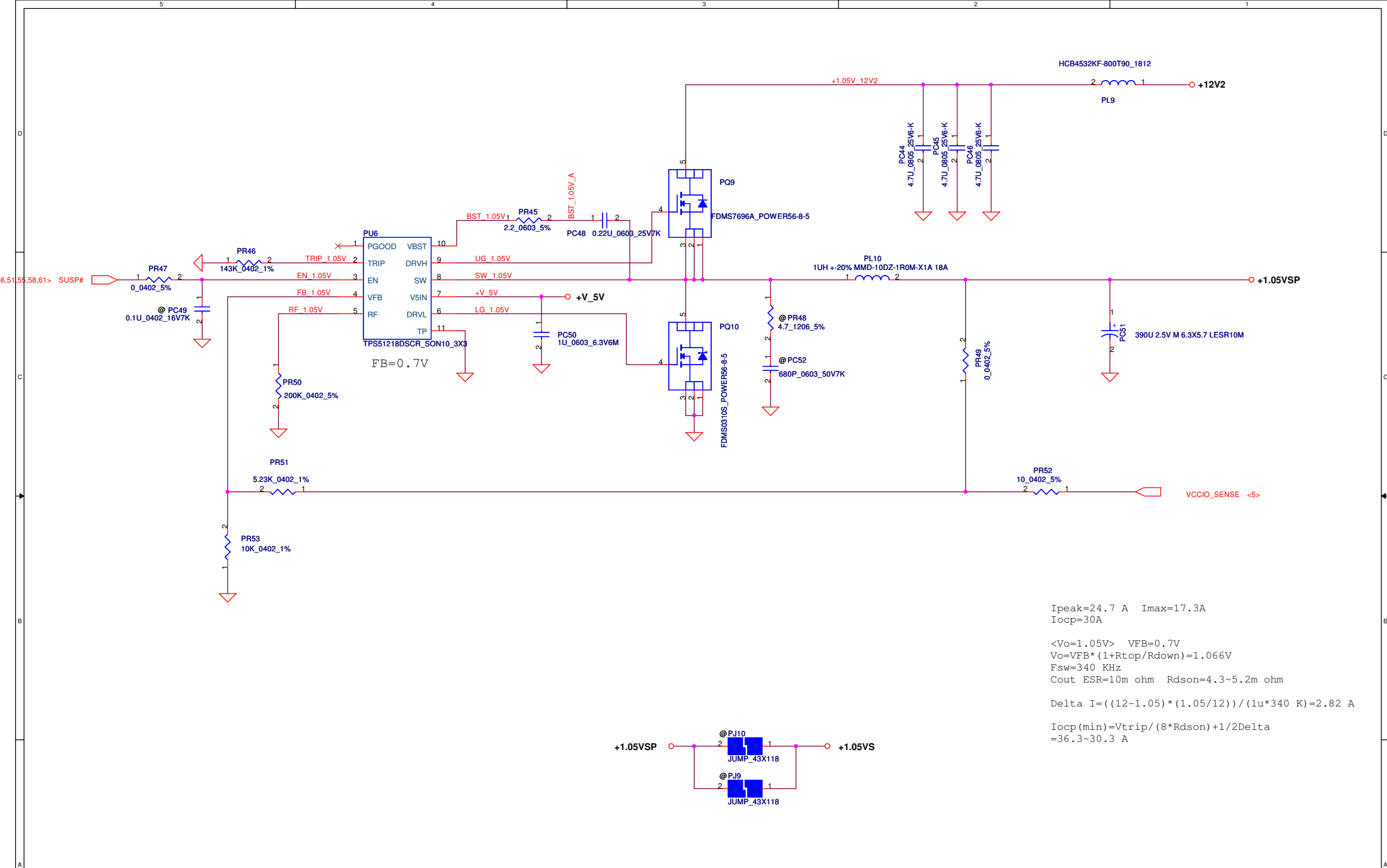
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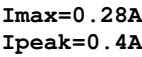
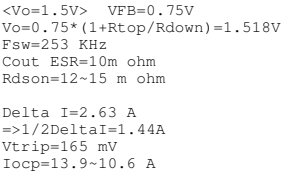
VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)



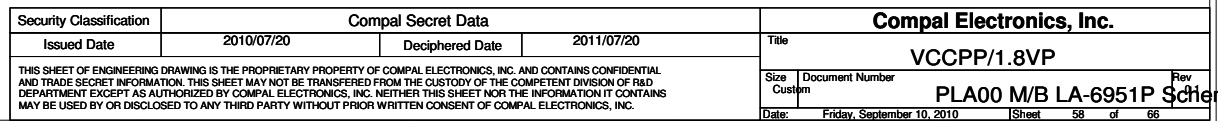
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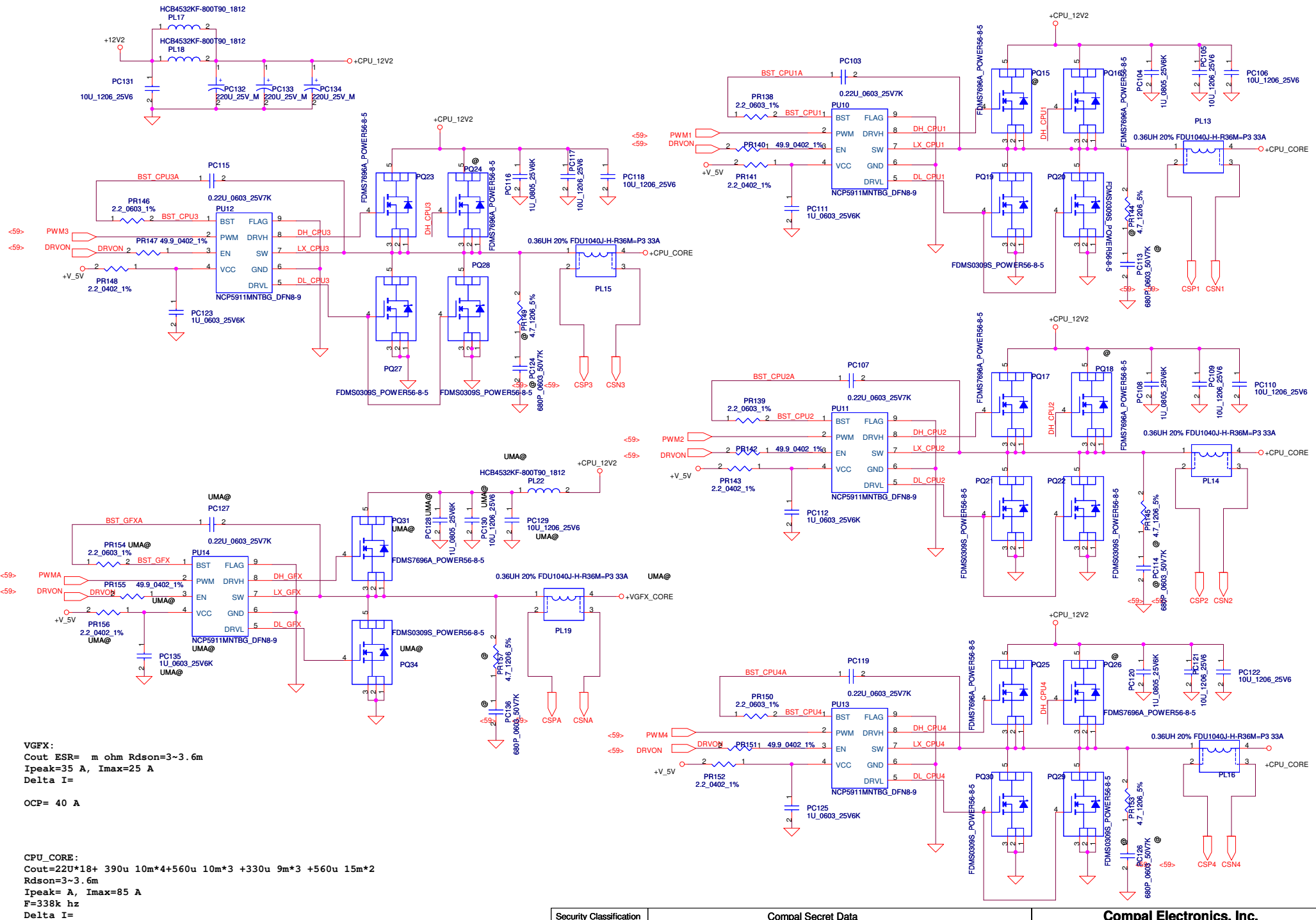


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			A
Title			<Title>
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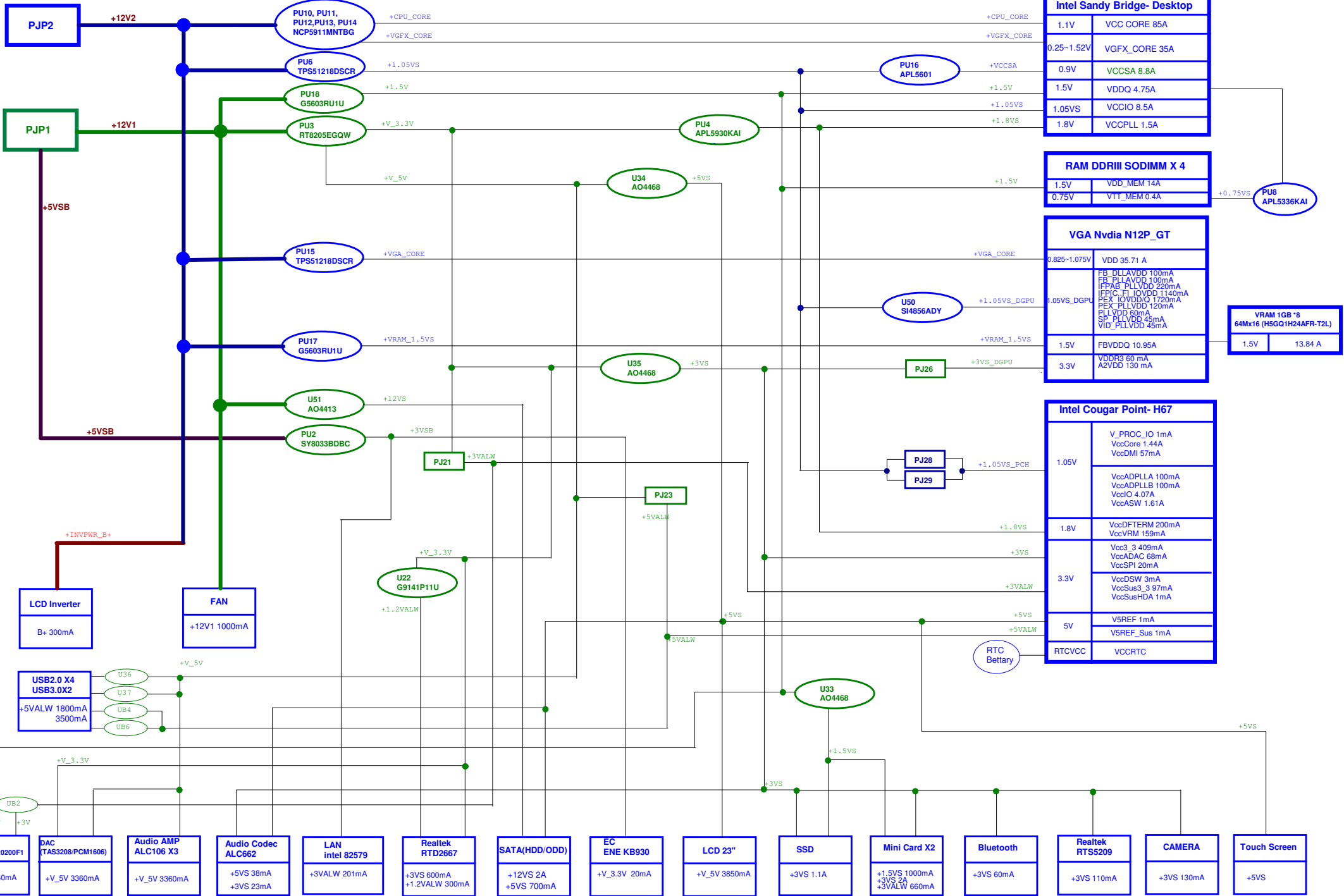
5

4

3

2

1



Intel Sandy Bridge- Desktop	
1.1V	VCC CORE 85A
0.25~1.52V	VGFX_CORE 35A
0.9V	VCCSA 8.8A
1.5V	VDDQ 4.75A
1.05VS	VCCIO 8.5A
1.8V	VCCPLL 1.5A

RAM DDRIII SODIMM X 4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 0.4A

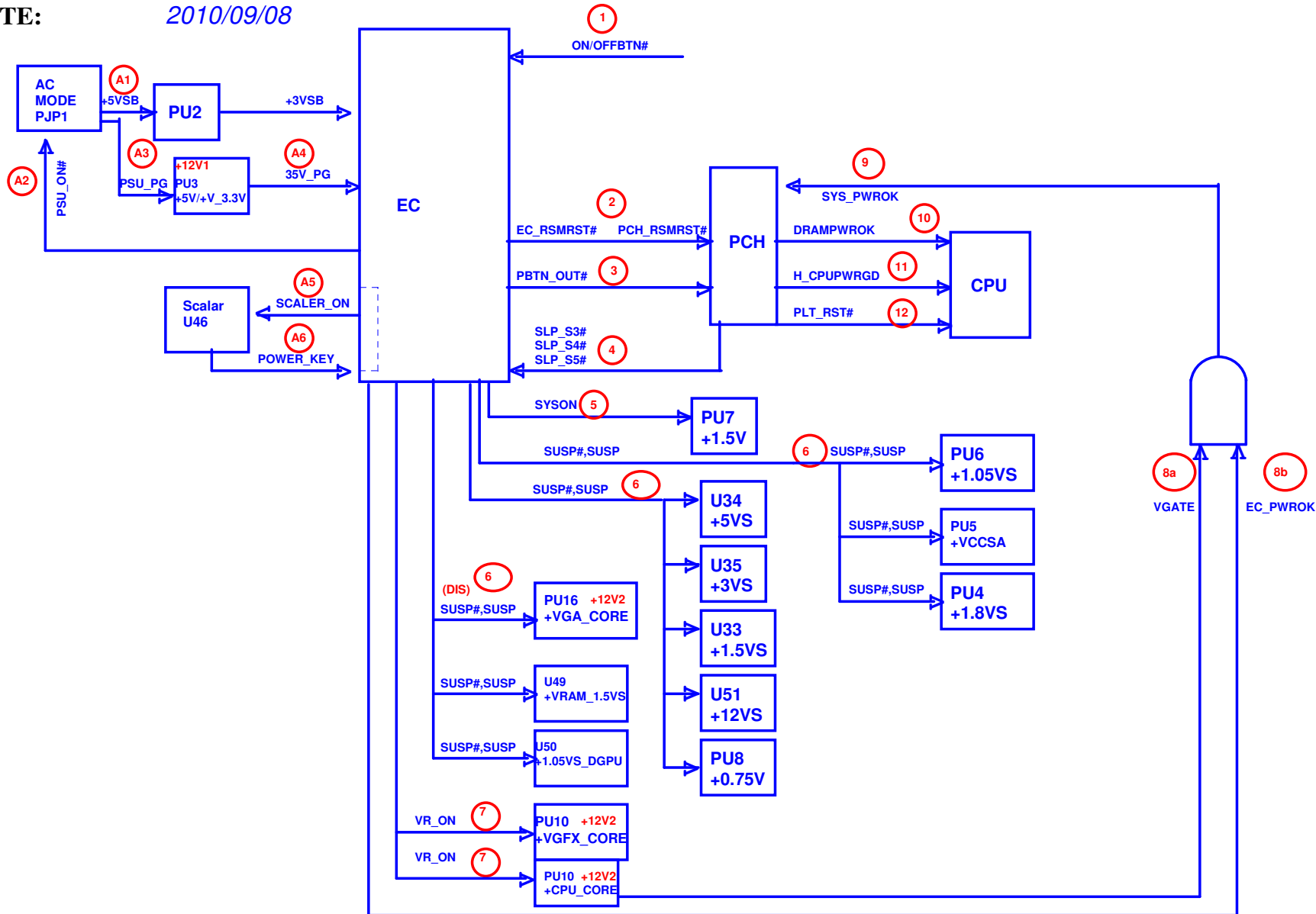
VGA Nvidia N12P_GT	
0.825~1.075V	VDD 35.71 A
	FB DLLAVDD 100mA FB PLLAVDD 100mA IFPAB PLLVDD 220mA IFPAB PLLVDD 1140mA PEX IOVDDQ 1720mA PEX PLLVDD 120mA PLLVD 60mA SP PLLVDD 45mA VID PLLVDD 45mA
1.05VS_DGPU	
1.5V	FBVDDQ 10.95A
3.3V	VDDR3 60 mA A2VDD 130 mA

VRAM 1GB *3 64Mx16 (H5GQ1H24AFR-T2L)	
1.5V	13.84 A

Intel Cougar Point- H67	
1.05V	V_PROC_IO 1mA VccCore 1.44A VccDMI 57mA VccADPLLA 100mA VccADPLLB 100mA VccIO 4.07A VccASW 1.61A
1.8V	VccDFTERM 200mA VccVRM 159mA
3.3V	Vcc3_3 409mA VccADAC 68mA VccSPI 20mA VccDSW 3mA VccSus3_3 97mA VccSusHDA 1mA
5V	V5REF 1mA V5REF_Sus 1mA
RTCVCC	VCCRTC

COMPAL CONFIDENTIAL

MODEL NAME: *PLA00 Power Sequence Block Diagram*
PCB NAME: *LA6951P*
REVISION: *0.1*
DATE: *2010/09/08*

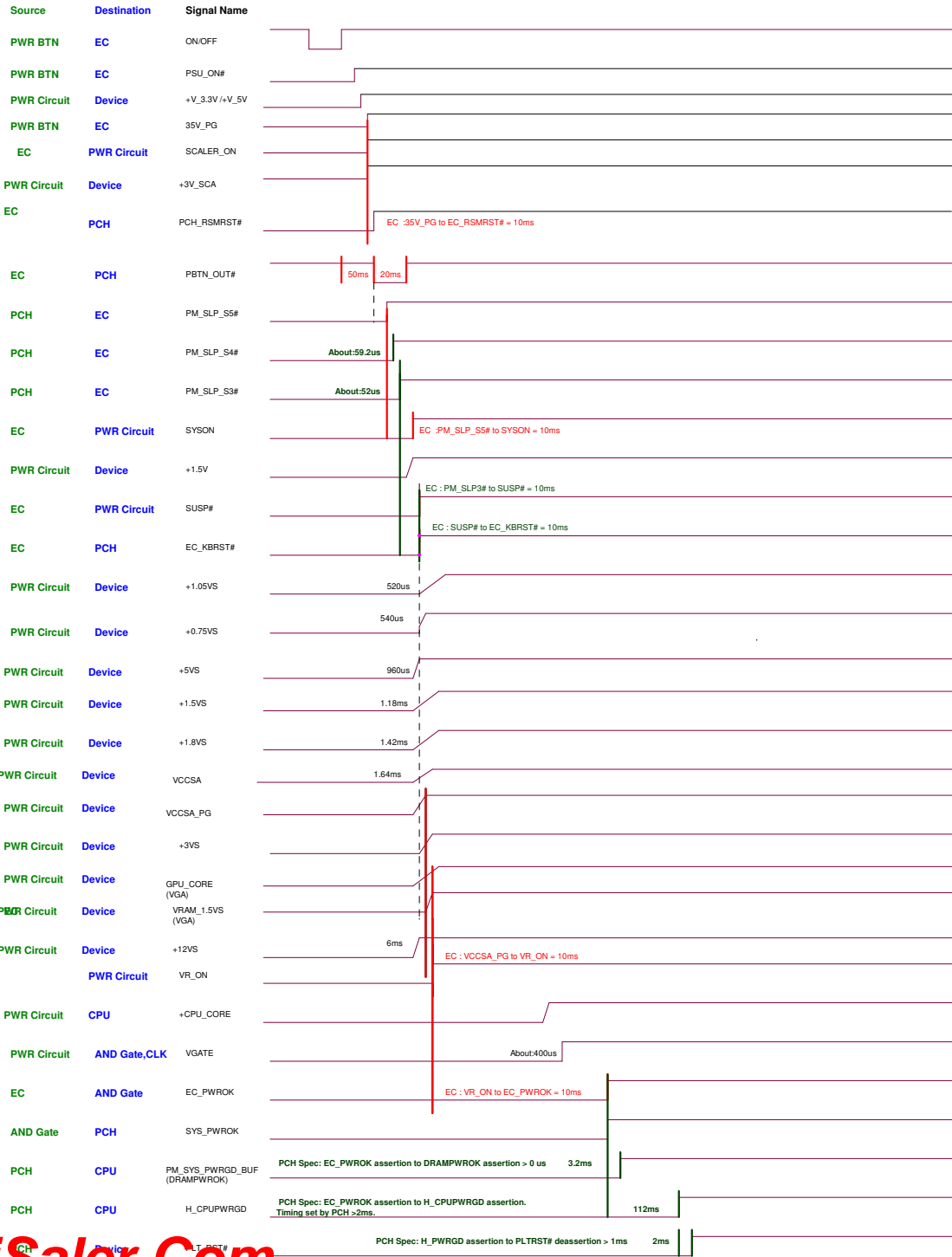


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B520 (OS S5)

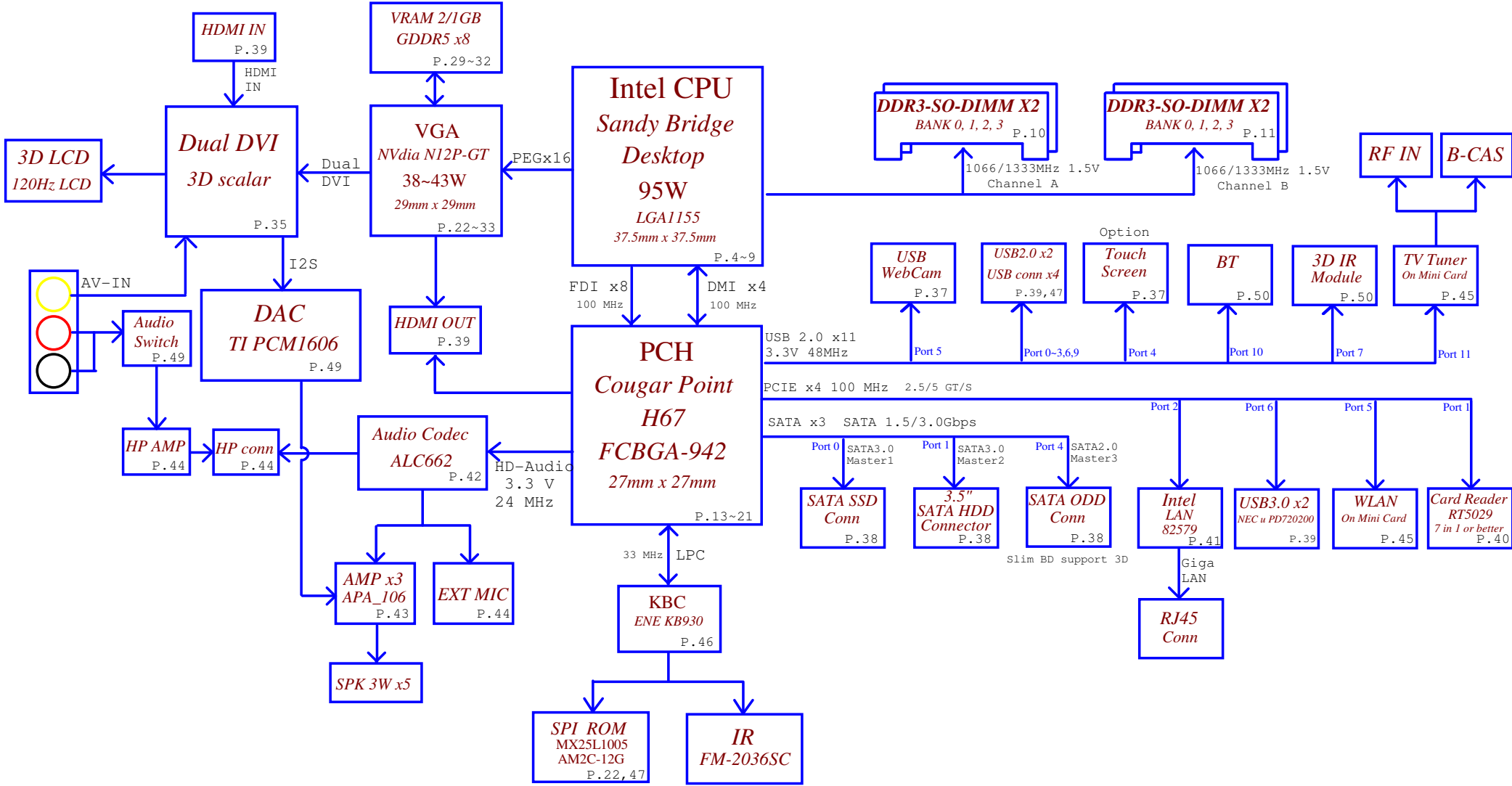
Power On
S5->S0

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Issued Date	2010/07/20	Disagreed Date	2011/07/20	Power Sequence	
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Model Name : PLA00
File Name : LA6951P



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